The present invention concerns principally a graphic display device.

Display devices of a known type store whole pictures in video memory, which requires a large memory capacity.

Working in front of display devices is becoming more and more frequent. For example, computer terminals comprise a cathode ray display device. Since the time spent in front of the display device is increasing, there is an incentive to improve the quality of the display in order to increase viewing comfort. This is particularly important in the case where important decisions have to be taken as a function of the data displayed. The display quality becomes critical for flying aircraft by instruments, measurements being displayed on cathode ray tubes (CRTs).

The device according to the invention is particularly sophisticated in displaying three-dimensional perspective views on a screen. The device according to the invention uses directed-beam scanning for drawings of the patterns of boundaries or symbols associated with frame scanning by which coloured zones can be obtained.

From the document IEEE Transactions on Computers, Vol. C-28, no. 7. July 1979, pages 528-531, a graphic display device is known comprising a colour screen of the frame scanning type; the display is obtained by filling in shadow regions having boundaries. The device comprises a microprocessor which calculates successively, for each frame line, the points of intersection of the frame line and the boundaries of the shadow regions; processing takes place frame by frame and the results obtained for a frame are stored in a video frame memory; such a memory has to have a large capacity, and is therefore expensive, bulky and heavy.

Other documents such as the article in IEEE Transactions on Computers, Vol. C 43, no. 7, July 1985, pages 666-673, which describes a device for filling in coloured zones, or European patent application 0 145 821, or the article in IBM Technical

Disclosure Bulletin, Vol. 27, no. 10B, March 1985, pages 6060-6061, present display devices in which processing takes place by frames and therefore, as in the first document cited, requires a large memory capacity.

The device according to the invention comprises a fast microprocessor calculating in real time, for each frame, the abscissa at the beginning and end of the display of each colour. By using a fast microprocessor calculating in real time the data displayed for each line, the size of the video memories used can be reduced considerably. This advantage is particularly important for equipment intended in particular to be loaded on aircraft where there is little space and where the weight of equipment loaded is a determining factor.

According to the invention, a graphic display device is proposed comprising a colour screen of the frame scanning type, the display being obtained by filling in coloured zones delimited by boundaries, comprising a microprocessor which calculates successively for each frame line the points of intersection of said frame line and said boundaries of the coloured zones, characterised by line-by-line processing of the picture and by the fact that it comprises for this purpose a video line memory storing one line of frames to be displayed and one only.

It will be easier to understand the invention by means of the following description and the annexed figures given as non-limitative examples, amongst which:

- Figure 1 is a drawing of a display screen;
- Figure 2 is a simplified drawing of patterns to be drawn on the screen;
- Figure 3 is a drawing of the various colour zones to be displayed;
- Figure 4 is a diagram of the device of a known type;
- Figure 5 is a drawing of colour zones to be displayed;

- Figure 6 is a diagram illustrating the coding of the colours in Figure 5;
- Figure 7 is a diagram of the content of the line memory corresponding to the coding in Figure 6;
- Figure 8 is a diagram of the device according to the invention;
- Figure 9 is a diagram of a production detail of the device according to the invention;
- Figure 10 is a drawing of a displayed picture;
- Figure 11 is a flow chart of the program used by the device according to the invention;
- Figure 12 is a flow chart of a subroutine of the program in Figure 11.

In Figures 1 to 12 the same references have been used to denote the same elements.

In Figure 1, an example can be seen of a drawing whose appearance on the screen 1 aids the pilot when landing an aircraft. The drawing comprises a simplified diagram of landing strips 200 as well as a tunnel 6 which corresponds to the optimised landing trajectory for the aircraft. The drawing comprises a view of the sky 2, and the land 3. The landing strip 200 comprises a central zone 5 corresponding to the place where the aircraft can land most safely as well as a peripheral zone 4. The tunnel 6 comprises four faces 7, 8, 9 and 10. The device according to the invention will draw by directed-beam scanning, for example on a CRT, the patterns corresponding to the horizon, the boundary between the sky 2 and the land 3, the boundaries 22, 23, respectively of the zones 4 and 5 of the landing strip 200 as well as the visible edges of the tunnel 6. Directed-beam scanning allows a drawing which is very clear and very easy for the pilot to perceive and interpret. The device according to the invention will make viewing more comfortable by colouring in different colours the sky 2, and land 3, the zones 4 and 5 of the landing strip 200 and the corridor 6.

With advantage, the device according to the invention receives from a picture synthesiser the data on the hidden faces of three-dimensional objects such as for example the landing tunnel.

From this information, the device according to the invention is capable of colouring with only the colour visible at each point of the screen. Filling in with colours takes place by frame scanning, faster than directed-beam scanning.

Figure 2 shows on the screen 1 the pattern drawn by directed-beam scanning corresponding to the horizon 21 and the boundaries 22 and 23 respectively of the zones 4 and 5 of the landing strip 200. For clarity of the drawing, the corridor 6 has not been drawn on Figure 2. Directed-beam scanning with a shadow-mask tube is carried out in a known manner.

In Figure 3, it can be seen how the sky 2, the land 3 and the zones 4 and 5 of the landing strip 200 have been filled in in colour. The colouring of zones 2 to 5 is carried out by frame scanning during the periods not used for directed-beam scanning by the tube. For example, a period of directed-beam scanning of 8 ms is succeeded by a period of frame scanning of 8 ms, and so on.

Figure 4 shows a device for displaying a synthesised picture on a CRT of known type. This device comprises a graphic processor 12 associated with a display memory 14. The display memory 14 is connected to a video processor 15 directly controlling the red, green and blue electron guns 16 of the shadow-mask CRT, not shown. A frame scanning circuit 13 is connected to the graphic processor 12 and the video processor 15. The graphic processor 12 receives via a bus 11 the pictures generated by a surface symbol generator [GSS = générateur de symbole surfacique in French]. It displays them in the display memory 14. The display memory is a memory comprising several arrays allowing storage of the information necessary for constituting a whole picture. Writing the display memory comprising a whole picture requires very powerful graphic processors.

With advantage, the device of prior art uses a display memory comprising two pages 17 and 18. The graphic processor writes one of the memory pages 17 or 18 alternately, the other one 18 or 17 serving to generate the desired picture on screen. The graphic processor 12 is connected by a bus 19 to the memory pages 17 and 18. The memory pages 17 and 18 are connected by a bus 20 to the video processor 15. The frame scanning circuit 13 makes it possible to synchronise the addressing of the pages in the display memory 14 with the display. The frame scanning circuit 13 comprises counters. The video processor 15 generates analogue signals by which the electron guns of a colour CRT may be directly controlled. The signals 16 driving the red, green and blue guns make it possible to obtain the desired colours.

Figure 5 shows an example of the figures to be displayed on the screen 1. The same scale has been used in Figures 5, 6 and 7. The picture to be displayed comprises surfaces 24, 25, 26, 27 and 28 in different colours. The surfaces are considered to be closed surfaces, in some cases closed by the edge of the screen 1. In some cases the surface of one colour covers part of the surface of another colour, for example the portion 270 of the surface 27 is covered by the surface 26. Similarly, the portion 260 of the surface 26 is covered by the surface 28.

The device according to the invention processes in real time each line to be displayed. Let us take for example the line 30. It intersects the surface 25 at the point 31 and at the point 310. The line 30 intersects the surface 28 at the point 32. The line 30 intersects the surface 26 at the points 33 and 35. The line 30 intersects the surface 27 at the points 34 and 310. The line 30 does not intersect the surface 24.

Figure 6 shows the timing diagrams corresponding to the display of the various colours on the line 30 in Figure 5. A high logic state corresponds to the presence of the colour; a low logic state corresponds to the absence of colour. The curves 25, 26, 27 and 28 represent the presence or absence of colours on the surfaces 25, 26, 27 or 28 on the line 30 in Figure 5. The curve

36 shows the coding resulting from the colours to be displayed for the line 30 carried out by the microprocessor of the device according to the invention. This coding has been carried out taking into account colour priorities resulting from the existence of a drawing of hidden faces located behind the visible faces. Thus, for example the region 270 of the surface 27 hidden by the surface 26 will not appear on the screen.

Figure 7 shows the filling of a video line memory in which are recorded the presence and absence of the various colours. This memory comprises as many words as there are colours to be displayed. For example the video line memory comprises sixteen words. The length of the word expressed in bits corresponds to the number of picture elements (pixels). For example, for a small tube comprising 256 pixels, words of 256 bits are used. The words 37, 38, 39, 40 and 41 correspond respectively to the colours of surfaces 28, 26, 27, 25, etc. In the memory word of a given colour, a "1" is recorded at the address corresponding to the number of the pixel where the boundary of said colour is crossed on the line 30. With advantage, a "1" is not marked for pictures going outside the screen and thus ending at the point 310 in Figure 5. Furthermore, there remain isolated "1"s corresponding to a singular point, for example, the point 32. This "1", being eliminated subsequently, is not shown in the figure. All the words corresponding to all the colours are read in parallel by lines 370, 380, 390, 400, 410 and so on.

Figure 8 shows the general arrangement of the device according to the invention. The device comprises a microprocessor 42 associated with a video line memory 45 and a video processor 15.

With advantage, the device comprises a register 47 and a decoder 43 connected by "exclusive OR" logic gates to the video memory 45 so that the singular points for which no colour change is desired can be processed.

With advantage, the device according to the invention comprises a second video line memory 46 associated with a register 48 and a

decoder 44 by "exclusive OR" logic gates 50. A frame scanning circuit 13 is connected to the microprocessor 42 and to the video processor 15. The microprocessor 42 receives via a bus 11 the digitised data on the picture to be displayed. This data originates from a picture synthesiser 810, a digital optical disk or an analogue-to-digital converter connected to a video cassette recorder or a television camera. The microprocessor 42 is connected via a bus 191 to the decoders 43 and 44. The bus 191 transmits the priorities assigned to the various colours which it is desired to be able to display. The microprocessor 42 is connected via an address bus 190 to the memories 45 and 46. The memories 45 and 46 are connected by a bus 211 to the video processor 15. On the other hand, the bus 211 connects the memories 45 and 46 to the registers 47 and 48 respectively. The registers 47 and 48 are connected to the memory 45 by the intermediary of the same "exclusive OR" circuits 49 and 50 as the decoders 43 and 44 respectively. The microprocessor 42 is associated with a random access memory (RAM) 420. The microprocessor 42 is connected to the memory 420 by the intermediary of a data bus 422, a control bus 421 and an address bus 423.

With advantage, the microprocessor 42 comprises an internal RAM replacing the RAM 420. For example the TMS 320 microprocessor sold by Texas Instruments comprises a fast internal memory of 144 16-bit words.

For each line of frame scanning, the microprocessor 42 calculates the coordinates of the intersection between the scanning line and the boundaries of the surfaces to be coloured. In Figure 5, such points of intersection bore the references 31, 32, 33, 34, 35, 310. The display on the screen comprises two stages. In an initial stage, the outline of the picture bearing the references 21, 22 and 23 in Figure 2 is traced by directed-beam scanning. In a second stage the surfaces are coloured with the aid of frame scanning. During the first stage the microprocessor 42 stores the parameters defining the boundaries in the memory 420, in the form of a table. In the second stage the microprocessor 42 calculates for each boundary the coordinates of any intersection of

the boundary with the frame line. These intersections are stored as they occur in one of the two line memories, for example 45. The coordinates loaded in the memory 45 will serve to display the following line. Simultaneously, the other memory - the memory 46 in this case - allows a frame line to be displayed currently. With the following line, the role of the memories 45 and 46 has to be changed. The memory 46 is erased. The microprocessor 42 will write to the memory 46 the coordinates of the intersections of the boundaries with the line, whilst the memory 45 will be charged with displaying the line previously calculated.

In an example embodiment of the device according to the invention the video processor 15 comprises an assembly of n bistables 151, a priority encoder 152, a memory 153 and an interface 154. The assembly of n bistables 151 is connected to the bus 211. The bistables 151 are connected to an encoder 152 by n lines. The encoder 152 is connected by an address bus to the memory 153. The memory 153 is for example a random-access memory (RAM). The memory 153 is connected by a data bus to the interface 154. The interface 154 is connected by analogue lines 16 for example to electron guns by which the red, green and blue colour can be delivered to a colour CRT 311.

The circuit 151 comprises as many bistables as there are colours to be displayed. The bus 211 transmits in parallel the data on the n colours which it is desired to be able to display, for example 16. In this case each of the sixteen bistables 151 changes state each time a boundary has been detected for a colour, that is when "1" is present at its input. Thus, the bistables 151 generate the marker pulses 23 to 28 in Figure 5. These marker pulses allow the encoder 152 to generate the marker pulse address, the palette memory 153, in which are stored the combinations of intensities of the red, green and blue colours necessary for obtaining each desired colour. The encoder 152 takes account of the priorities for displaying colours. The colours obtained are illustrated by the curve 36 in Figure 6. In fact, the encoder 152 generates over the time desired, within the scanning of one frame line, the address in the palette memory 153

of the desired colour, then generates the following colour and so on until the end of the frame line. In the example illustrated by the curve 36 in Figure 6 the encoder 152 generates the address in the memory 153 of the colour of the region 25, that of the region 26, then that of the region 27.

In a first embodiment of the device according to the invention, the hierarchy of priorities is hard-wired within the encoder 152. Logic gates block the generation of the address in the memory 153 of a colour if a colour placed higher in the hierarchy of priorities also has to be displayed.

In a second variant embodiment of the device according to the invention, a programmable encoder is available which makes it possible to change the order in the hierarchy of priorities. In this case, the encoder 152 receives via a bus not shown in Figure 8 the desired order of hierarchy.

The bus connecting the encoder 152 to the memory 153 is for example a 4-bit bus allowing the screen to generate sixteen colours. The palette memory 153 delivers the digital values of the intensities of the primary colours necessary for obtaining the desired colours. For a random-access palette memory 153 the colours can be changed by loading, via a bus not shown, the new values of combinations of red, green and blue primary colours by which said colours may be obtained. The interface 154 consists for example of three digital-to-analogue converters, driving either directly or by the intermediary of an amplifier - not shown - the electron guns of a CRT 311.

In another variant embodiment, the memory 153 is a permanent memory, for example a programmable read-only memory (PROM), an electrically programmable memory (EPROM) or an electrically reprogrammable read-only memory (EEPROM). In this case it is advantageous to preload the desired colours.

It may be appreciated that the video processor 15 is suited to a screen comprising an RVB-type video interface, such as for

example a colour CRT, an electroluminescent screen or a colour liquid crystal screen. It may be appreciated that if a directly addressable matrix screen is available the video processor 15 and particularly the interface 154 will be suitable for addressing this type of screen.

In Figure 9, a detail can be seen of an embodiment of the device in Figure 8. The diagram in Figure 9 makes it possible to explain the management, by a system according to the invention, of a singular point, that is, a single point [of] intersection of the scanned line with a surface. The point 32 on Figure 5 and also the point 73 on Figure 10 are singular points. The device in Figure 9 makes it possible to avoid changing colour at a singular point. The memory is organised in n words of for example 256 bits. n is the number of colours that it is desired to display simultaneously on the screen, 256 is an example of the number of pixels which it is desired to be able to display on each line. It may be understood that the invention applies to different number of colours and numbers of pixels. For example, for a computer-aided design (CAD) workstation, a display of 1024 lines will be used, comprising 1024 pixels which can take 128 colours. Before writing a line the video memory 45 is erased, that is, loaded with zeros at all addresses. For each intersection of the colour boundary with the frame line a "1" is recorded for each of the colours at the coordinate of said intersection. In each of the words corresponding to a colour, writing takes place bit by bit. There is therefore no need for a data bus - two address buses 190 and 191 are simply used. The bus 190 transmits the coordinate in which writing must take place, and the bus 191 transmits to the decoder 43 the colours for which it is desired to write a "1". The last point recorded is transmitted by the bus 211 to the register 47. Each of the colours coming from the register 47 is connected by one of the "exclusive OR" logic circuits 49 to the colour inputs to the memory 45. The other input of the "exclusive OR" logic circuits 49 is connected to the colour decoder 43. At a singular point, the decoder 43 had for the colour(s) concerned the order to write a "1" corresponding to the second intersection of the boundary of

the colour(s) with the frame line. Given that the register 47 stored the previous transition there will be a "1" at both inputs of the "exclusive OR" circuits 49. Thus the logic circuit 49 will furnish a "0" to the video memory 45. Similarly, if no intersection should be recorded either at the previous writing, or at the current writing, then the circuit 49 will furnish a "0". On the other hand, if a "1" corresponding to an intersection is written at just one of the two successive writings, the "exclusive OR" circuit 49 will furnish a "1" at its output, having a "0" at one of its inputs and a "1" at the other one of its inputs.

Synchronisation of the video memory 45 and the register 47, or the video memory 45 and the register 48 is carried out by read/write signals 162. These signals allow alternately reading of the memory 45 and writing of the register 47 or writing of the memory 45 and reading of the register 47. The read/write to write/read control signals 162 of the video memory 45 and the register 47 are generated either by microprocessor 42 or by an external logic of known type, not shown.

In Figure 10, an illustration is given of an example of a screen 1 which it might be desired to display, the resulting display and the calculation to be effected for two frame lines 60 and 70. The screen 1 in Figure 10 comprises surfaces 81, 82, 83, 84, 85 and 86. As can be seen in the figure the surface 81 has the lowest priority, and indeed is covered by each of the surfaces 82 to 86. It can be seen on the other hand that the surface 83 has a lower priority than the surfaces 84, 85 and 86. Thus each time it is necessary to colour part of the screen covered by the surface 83 and for example the surface 84, it will be coloured with the colour corresponding to the surface 84. It is also seen that the surface 84 has a lower priority than the surface 85.

In Figure 10, two frame lines referenced 60 and 70 have been taken in an arbitrary fashion to explain the functioning of the device according to the invention. In reality the display of a screen is obtaining by directed-beam scanning of the patterns and

frame scanning of all the frame lines of the screen 1. In Figure 10, the first boundaries of a colour have been represented by black points and the second boundary of a colour by crosses. The point 61 corresponds to the intersection of the first boundary of the surfaces 81 and 82 with the line 60. The point 62 corresponds to the second boundary of the surface 82 with the line 60. The point 63 corresponds to the first boundary of the surface 83 with the line 60. The point 64 corresponds to the first boundary of the surface 84 with the line 60. The point 65 corresponds to the first boundary of the surface 85 with the line 60. The point 66 corresponds to the second boundary of the surface 84 and the line 60. The point 67 corresponds to the intersection of the second boundary of the surface 85 and the line 60. The point 68 corresponds to the intersection of the second boundary of the surface 83 and the line 60. The point 69 corresponds to the second boundary of the surface 81 and the line 60.

The point 71 corresponds to the intersection of the first boundary of the surface 81 with the line 70. The point 72 corresponds to the intersection of the first boundary of the surface 83 with the line 70. The point 73 corresponds to the first and second boundaries of the surface 86 with the line 70.

The point 73 is a singular point. A clear display on the screen demands that the colour of this point should not be changed during frame scanning. The singular point processing carried out by the "exclusive OR" logic circuits 49 and 50 in Figures 8 and 9*.

The point 74 corresponds to the intersection of the first boundary of the surface 85 and the line 70. The point 75 corresponds to the first boundary of the surface 84 and the line 70. The point 76 corresponds to the second boundary of the surface 85 and the line 70. The point 77 corresponds to the intersection of the second boundary of the surface 84 and the line 70. The point 78 corresponds to the intersection of the second boundary of the surface 83 of the line 70. The point 79 corresponds to the intersection of the second boundary of the surface 81 and the line 70.

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* Translator's note: There is no main verb in this sentence in the original.

Figure 11 shows a flow chart of the processing program carried out by a microprocessor 42. The program in Figure 11 is a programmable rotating continuously throughout the display on the screen. The program starting at 91. At that time the microprocessor receives an interrupt 90 of the synchro-frame signal. After this interrupt allowing the calculation to be synchronised with the scanning of the screen, go from 91 to 92. At 92, store data concerning the display to be made in the memory 420. From 92, go to 93 which corresponds to the end of storing data in the memory 420. The data is for example stored in the form of a table of the boundaries comprising the line at the beginning of a boundary as well as the equation defining this boundary. For this type of data organisation, no boundary comprises more than one intersection with any of the frame lines. Thus to define a closed zone to be coloured at least two boundaries are needed.

If all the boundaries are straight lines, it is sufficient to store the slope of each straight line in the table in the memory 420, the general equation of all the straight lines being identical.

These stages correspond for example to half the program time carried out by the microprocessor including the waiting times for synchronisation.

In an example embodiment of the device according to the invention the executive of part 91 to 93 of the program lasts 8 ms.

From 93, go to 94. At 94, wait for the synchro-line interrupt 95. This interrupt triggers the start of the calculation of the intersections of the boundaries of the surfaces with the frame line processed. From 96, go to 97. At 97, test whether the line processed is the last line of the frame. If no, return to 94 and wait for the synchro-line interrupt which will trigger the calculation of the intersections 96 of the following line. If yes, return to 91 and await the interrupt 90 of the synchro-frames. The second part of the program from 94 to 97 also lasts, in a

particular example of an embodiment of the device according to the invention, 8 ms.

Figure 12 shows a flow chart of a subroutine for calculating the intersections in the program in Figure 11. This subroutine corresponds to step 94 to 97 in Figure 11.

The subroutine corresponds to the case where the boundaries of the various surfaces are straight lines. All the surfaces which can be displayed on the screen are approximated by series of straight lines. In another case it is possible to define other types of surface boundary comprising straight lines, arcs of a circle, ellipses and hyperbolas. Of course, the type of boundaries used must be defined in order to allow calculation in the microprocessor 42 in Figure 8.

The subroutine in Figure 12 starts at 144. At 144, set the counter of the number L of the line processed to "0". Go to 98. At 98 an interrupt 95 of the synchro-line is received, which starts the calculation. L is increased by one unit. From 98 go to 197.

At 197, set the boundary index i to "0".

Go to 196.

At 196, increment the boundary index i by one unit. Go to 99. At 99, test whether the line L processed currently intersects the boundary yi. This data is read in a table contained by the memory 420 in Figure 8.

If no, go to 103.

If yes, go to 100.

At 100 write the intersection x_i in the memory line 45 or 46. Go to 101.

At 101, check whether the boundary yi finishes at the point of intersection of the memory 420 in Figure 8.

If yes, go to 103.

If no, go to 102.

At 102, record in the table of the memory 420 in Figure 8 that the boundary previously processed intersects the lower frame line. Go to 195.

At 195, calculate and store in a table [of] the memory 420 in Figure 8 the abscissa of the boundary previously processed one line lower down. Go to 103.

From 103, go to 104.

At 104, test whether the intersections for all the boundaries stored in the table of the memory 420 in Figure 8 have now been calculated. If no, go to 196. If yes, go to 105 which corresponds to the end of the subroutine. The execution of the subroutine in Figure 12 has lasted for example 8 ms.

The device according to the present invention applies principally to high-quality colour display. The invention applies particularly to the display on a colour CRT screen of three-dimensional perspective views.

CLAIMS

1. A graphic display device comprising a colour screen (1) of the frame scanning type, the display being obtained by filling in coloured zones (2, 3, 4, 5, 7, 8, 9, 24, 25, 26, 27, 28, 81, 82, 83, 84, 85, 86) delimited by boundaries (21, 22, 23), comprising a microprocessor (42) which calculates successively for each frame line (30, 60, 70) the points of intersection (31, 32, 33, 34, 35, 310, 61, 62, 63, 64, 65, 66, 67, 68, 71, 72, 73, 74, 75, 76, 77, 78, 79) of the next frame line to be displayed (30, 60, 70) with said boundaries (21, 22, 23) of the coloured zones (2, 3, 4, 5, 7, 8, 9, 24, 25, 26, 27, 28, 81, 82, 83, 84, 85, 86), characterised by line-by-line processing of the picture and by the fact that it comprises for this purpose a video line memory (45 or 46) storing one line of frames to be displayed and one only.

2. A device according to Claim 1, characterised by the fact that the boundaries (21, 22, 23) of the coloured zones (2, 3, 4, 5, 7, 8, 9, 24, 25, 26, 27, 28, 81, 82, 83, 84, 85, 86) are drawn on the screen by directed-beam scanning.

3. A device according to Claims 1 or 2, characterised by the fact that the screen (1) is a colour cathode ray tube (311) of the planar mask type.

4. A device according to Claim 3, characterised by the fact that it comprises two video memories (45 and 46), one (45 or 46) alternately allowing the writing of data to be displayed on the following frame line, the reading of the other (45 or 46) allowing a frame line to be displayed.

5. A device according to Claim 3 or 4, characterised by the fact that it comprises a register (47, 48) connected to the output of each video memory (45, 46) and "exclusive OR" logic gates (49, 50) connected between the input of the memory (45, 46) and the register (47, 48) on the one hand and the microprocessor (42) on the other hand, making it possible to avoid

inscribing in the video memory (45, 46) the existence of a multiple intersection at a point between a frame line (30, 60, 70) and a boundary (21, 22, 23) of coloured zones (2, 3, 4, 5, 7, 8, 9, 24, 25, 26, 27, 28, 81, 82, 83, 84, 85, 86).

6. A device according to any one of the preceding claims, characterised by the fact that said device is a device for displaying three-dimensional views in perspective.

7. A device according to any one of the preceding claims, characterised by the fact that that it comprises a video processor (15) including a palette memory (153) in which are stored the intensities of the primary colours necessary for obtaining the desired colours associated with an interface comprising a digital-to-analogue converter associated with each primary colour generator.

8. A device according to any of Claims 3 to 7, characterised by the fact that the video memory (45, 46) is organised in n words in which the number of bits is equal to the number of picture elements per frame line, n being the maximum number of colours that can be used.

9. A device according to Claim 8, characterised by the fact that it comprises bistables (151) connected in parallel to the output of each word of the video memory (45, 46) each bistable changing its logic state when it receives a "1", the bistables (151) being connected to a priority encoder (152) which is itself connected to the palette memory (153).

10. A process for graphic display on a screen (1), comprising the following steps:

- directed-beam scanning allowing the boundaries (21, 22, 23) of zones to be displayed;
- frame scanning of coloured zones (2, 3, 4, 5, 7, 8, 9, 24, 25, 26, 27, 28, 81, 82, 83, 84, 85, 86), using a micro-processor (42) to calculate successively, for each frame line (30, 60, 70), the points of intersection (31-35, 310, 61-69,

71-79) of said frame line with the boundaries of the coloured zones, characterised by line-by-line processing of the picture and by the fact that, for this purpose, during the frame scanning stage one line is displayed by reading a memory (420) and simultaneously a calculation is made and stored in the memory (420) by the microprocessor (42) of the abscissas of the points of intersection (31, 32, 33, 34, 35, 310, 61, 62, 63, 64, 65, 66, 67, 68, 69, 71, 72, 73, 74, 75, 76, 77, 78, 79) of the next frame line to be displayed with the boundaries (21, 22, 23) of the coloured zones (2, 3, 4, 5, 7, 8, 9, 24, 25, 26, 27, 28, 81, 82, 83, 84, 85, 86) and that one frame line to be displayed and one only is stored in a video line memory (45 or 46).

11. A device according to Claim 10, characterised by the fact that the boundaries (21, 22, 23) of the coloured zones (2, 3, 4, 5, 7, 8, 9, 24, 25, 26, 27, 28, 81, 82, 83, 84, 85, 86) segments of a straight line.

12. A process according to Claims 10 or 11, characterised by the fact that said process is a process for displaying views in perspective of three-dimensional objects taking account of the hidden faces of said objects taking into account the priority colours of the overlap zones (260, 270) of two coloured zones (2, 3, 4, 5, 7, 8, 9, 24, 25, 26, 27, 28, 81, 82, 83, 84, 85, 86).

13. A display process according to Claims 10, 11 or 12, characterised by the fact that said process is a process for displaying a picture synthesised by a surface symbol generator (810).