ABSTRACT

METHOD OF MANUFACTURING A GATE STRUCTURE FOR A SEMICONDUCTOR MEMORY DEVICE WITH IMPROVED BREAKDOWN VOLTAGE AND LEAKAGE RATE

The invention is a method of manufacturing a semiconductor memory device using a novel intergate dielectric stack. A key feature of of the invention is the novel O/N/SiON/O structure, forming a silicon oxynitride layer on the silicon nitride layer. The method begins by forming a first insulating layer and a first conductive layer on a semiconductor substrate having one conductivity type. A second insulating layer is formed on the first conducting layer by sequentially stacking: a first silicon oxide layer; a silicon nitride layer; a silicon oxynitride layer; and a second silicon oxide layer. A second conductive layer is formed on the second insulating layer. The first insulating layer, the first conductive layer, the second insulating layer, and the second conductive layer are patterned to form a floating gate, an intergate dielectric, and a control gate. Finally, a source and drain are formed to complete the memory device.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)