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DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Process for Encapsulating Electronic Devices in Plastics and Devices so Produced

We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organised according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement: —

This invention relates generally to the manufacture of semiconductor devices, and more particularly, but not by way of limitation, relates to an improved process for fabricating semiconductor devices, such as transistors, for example, and to the product of the process.

In general, semiconductor devices are very small and delicate which makes the economical manufacture of high quality devices in a practical and usable form on a mass production basis very difficult. For example, such devices must have electrical leads sufficiently large that they can be easily soldered or otherwise connected by hand, or by automated equipment, into the final circuit. The devices must be sufficiently rigid to withstand handling, and for many applications must withstand high mechanical shock loads. Further, the components must be packaged so that the leads are electrically isolated. Further, the semiconductor wafers must be protected from some forms of radiant energy, such as light, and heat must be conducted away from the active regions of the device to maintain the device within its safe operating temperature range.

According to one aspect of the present invention there is provided a semiconductor device consisting of a plurality of lead wires forming all the connections to the device, the wires being side by side and substantially parallel for the greater part of their lengths, one end of at least one of the lead wires being flattened, a semiconductor wafer bonded to the flattened end of one of the lead wires, a wire bonded to the end nearest the semiconductor wafer of each of the other lead wires and to a contact in the semiconductor wafer, and a one-piece body of thermosetting plastics material encapsulating the connected ends of the lead wires, the semiconductor wafer, and the wires interconnecting the wafer and the ends of the lead wires, the connected ends of the lead wires terminating within the body of thermosetting plastics.

According to another aspect of the present invention there is provided a process for encapsulating a semiconductor device, comprising the steps of:

frictionally securing substantially parallel portions of a plurality of lead wires side by side in a carrier block with one end of each lead wire cantilevered out from the carrier block, one cantilevered end of a lead wire being flattened,

mounting a semiconductor wafer on the flattened end and electrically connecting the wafer to the cantilevered ends of the other lead wires,

encapsulating the cantilevered ends of the lead wires, the wafer and the electrical connections in a one-piece body of plastics material to seal the wafer in a stabilizing environment and mechanically rigidify the device, and

removing the lead wires from the carrier block.

An advantage of a process according to the present invention is that it reduces waste in metal and plastics materials and it decreases the number and complexity of the process

[*Price 5s. 0d.*]

steps of previous processes. The examples of a process according to the invention to be described are also particularly suited for increased automation, the process being useful in encapsulating substantially any semiconductor device, such as standard planar transistors, diodes, SCR's, as well as field effect transistors and MOS transistors for example, having any number of leads. Another advantage of a process according to the invention is that it may permit the fabrication of plastics encapsulated transistors in which the leads are arranged in a conventional circle pattern so as to be compatible with printed circuit boards set up to handle transistors packaged in a conventional hermetically sealed header and can assembly. More than one semiconductor device may be encapsulated in the same body of plastics material, with the semiconductor devices either separate or electrically interconnected.

Another important advantage of the invention is that the lead wires are protected throughout the fabrication process and during testing so that the leads of the final product are straight.

These and other advantages are achieved by mounting a plurality of lead wires in a carrier block which frictionally grips the lead wires and holds them in predetermined relationship with the ends of the lead wires cantilevered out from the block. A semiconductor device is then mounted on one of the cantilevered ends, the other ends electrically connected to the semiconductor device, and the ends and device encapsulated. In the fabrication of a transistor, for example, the three wires are disposed in parallel relationship. The cantilevered ends of the lead wires are then flattened to facilitate bonding the semiconductor wafer to one of the lead wires, to facilitate bonding of jumper wires between the wafer and the other leads, and to mechanically secure the wires in the final encapsulation body to increase the mechanical stability of the device. The cantilevered ends of the wires with the semiconductor wafer and whisker wires intact are then encapsulated in plastics material, preferably by placing the ends of the wires in a transfer mold cavity and injecting a thermosetting plastics material into the mold. The device may be tested while still held in the carrier block, and may then be easily removed from the carrier block. The carrier block can be used repeatedly.

The carrier block is comprised of a body of resilient material having a plurality of grooves for frictionally engaging the lead wires after the lead wires have been pressed into the grooves. The grooves may be arranged either in a common plane, or when three wires are used for a transistor or the like, the center groove may be raised in order to hold the three lead wires at the desired points on a circle, usually the corners of a right isosceles triangle, so as to position the lead wires in the same pattern as conventionally used for transistor devices encapsulated in a header and can assembly. The carrier blocks are adapted to be placed in side-by-side relationship on a handling tray, and to be easily aligned by indexing pins. The tray is designed so that the carrier blocks can be easily replaced, and the carrier blocks are designed so as to be reversible in the trays and therefore have a longer useful life. A multiple cavity mould can be employed and the process arranged for simultaneously encapsulating a plurality of the devices in a thermosetting plastic while using a minimum volume of plastic. This is achieved by aligning a plurality of the carrier blocks side-by-side in two rows with the lead wires extending toward the other row into two rows of mold cavities. Plastics is then forced down a single runner between the rows of cavities and through gates into each of the mold cavities to reduce the waste plastic.

The invention may best be understood by reference to the following detailed description of illustrative embodiments, when read in conjunction with the accompanying drawings, wherein:

FIGURES 1—6 are perspective views illustrating steps in the fabrication process of the present invention;

FIGURE 7 is a perspective view of a transistor fabricated by the process illustrated in FIGURES 1—6;

FIGURES 8—11 are perspective views similar to FIGURES 1—6 which illustrate an alternative embodiment of the process of the present invention;

FIGURE 12 is a perspective view of a transistor fabricated by the process illustrated in FIGURES 8—11;

FIGURE 13 is a plan view of a preferred embodiment of the carrier block used in the process illustrated in FIGURES 1—6;

FIGURE 14 is a side view of the carrier block of FIGURE 13;

FIGURE 15 is an end view of the carrier block of FIGURE 13;

FIGURE 16 is an end view of a preferred embodiment of the carrier block used in the process of FIGURES 8—11;

FIGURE 17 is a plan view, partially broken away to reveal details of construction, of a tray for a plurality of the carrier blocks illustrated in FIGURES 13—15;

FIGURE 18 is a sectional view taken substantially on lines 18—18 of FIGURE 17;

FIGURE 19 is a rear view of the tray illustrated in FIGURE 17;

FIGURE 20 is a plan view of the lower half of a multiple cavity mold constructed in accordance with this invention for carrying out the process of the present invention;

FIGURE 21 is a sectional view through

both the bottom and top halves of the mold illustrated in FIGURE 20;

FIGURE 22 is an enlarged sectional view of an individual cavity of the mold of FIGURE 20; and

FIGURES 23—26 are simplified drawings illustrating still another embodiment of the process of the present invention.

One embodiment of a process of the present invention is illustrated in FIGURES 1—6. A carrier block 10 is used to hold three lead wires 12, 13 and 14 in parallel relationship with the ends of the wires cantilevered out from the carrier block 10. The carrier block 10 is fabricated from a resilient material and is provided with parallel grooves 16, 17 and 18 for receiving the lead wires 12, 13 and 14 in a close interference fit so that the wires will be frictionally retained within the carrier block. This result is achieved by making the width of the grooves 16, 17 and 18 less than the diameter of the lead wires 12—14 and forming the carrier block 10 from a resilient material. The grooves also have a depth greater than the radius of the wires and preferably considerably greater.

The carrier block 10 is typically molded from a granular mixture of 25% glass and 75% TFE (polytetrafluoroethylene resin), although other materials having similar properties may be used. The glass-filled TFE can be molded to the necessary tolerances, and is sufficiently resilient to permit the lead wires to be forced into the grooves, yet rigid enough to retain its shape during repeated use. The glass-filled TFE also will withstand the temperatures encountered in the process steps which will presently be described.

The lead wires 12, 13 and 14 may be identical and are cut to the length required for the final device. The lead wires 12—14 are inserted in the grooves 16—18, respectively, by laying them in the tops of the grooves and then forcing them downwardly into the grooves by a wedge-shaped tool extending substantially the length of the lead wires and having a tip which will also pass into the grooves. Once forced into the grooves, the lead wires are frictionally retained therein against both rotational and longitudinal movement to a sufficient degree to carry out the remaining steps of the process, although both rotational and particularly longitudinal movement can be achieved by applying force.

Next, the ends of the wires 12—14 are inserted in a conventional press having dies which flatten the tips 12a, 13a and 14a of the wires substantially as illustrated in FIGURE 2. During this step, the ends of the wires may also be aligned at the proper distance from the end 10a of the carrier block 10 by abutting the carrier block 10 against a suitable stop while simultaneously abutting the ends of the wires against another appropriately located stop. Next, the ends of the wires are placed on a heater and small square of gold foil 20 placed on the flat end 13a of the center lead wire 13. The gold foil then melts and adheres to the lead. Next, a semiconductor wafer containing a device, e.g. a transistor 22 is placed on the gold foil and the lead wires heated so that the wafer is alloyed to the flattened portion 13a of the center lead 13 by the gold. In a transistor, this procedure usually connects the collector to the lead wire. A small diameter, gold whisker wire lead 24 is are then bonded to the expanded base contact on the wafer 22 and the flattened end 14a, and a lead 26 bonded to the expanded emitter contact and to flattened end 12a.

Next, the cantilevered ends of the leads 12—14, together with the transistor wafer 22 and jumper wires 24 and 26, are placed in a suitable transfer mold cavity and the ends of the lead wires 12—14 encapsulated by a body of plastic 28 as shown in FIGURE 6. After the device is removed from the mold, it can be tested, while still in the carrier block 10, by probes applied to the leads 12—14 because the carrier block 10 is an electrical insulator. The device may then be easily removed from the carrier block 10 by pulling on the plastic body 28 so as to move the leads longitudinally from the grooves 16—18. The finished device may appear substantially as illustrated in FIGURE 7, although the plastic material is opaque, not transparent as illustrated.

It will be noted that the lead wires 12—14 do not need to be trimmed at any stage of the process, so that no lead wire material is wasted, and there are no lead wires which must be sheared off at the plastic body and then coated with an insulator. The lead wires are securely anchored within the plastic capsule by reason of the flattened ends 12a—14a and cannot be rotated or pulled from the encapsulating body of plastic. Further, the ends of the lead wires ar spaced a substantial distance from the adjacent boundary of the encapsulating plastic and therefore are well insulated and protected from the ambient.

A process for fabricating a transistor in which the leads are oriented in the circle pattern conventionally used for hermetically sealed packages consisting of a metal header and a metal can is illustrated in FIGURES 8—11. In this process, a carrier block 30 is used to support lead wires 32—34 in parallel cantilevered fashion in parallel grooves 36—38 as heretofore described. The carrier block 30 may be molded from the same material as the carrier block 10 and the lead wires 32—34 retained by a friction fit in the grooves 36—38 as heretofore described. However, the bottom of the center groove 37 is disposed at a substantial height above the bottom of the two outer grooves 36 and 38 so that leads located in the bottoms of the grooves are oriented at the desired locations, which is

essentially the apexes of a right isosceles triangle.

The lead wires 33 and 34 may be of identical length and initially be perfectly straight so as to reduce inventory problems. Lead wire 32 is, however, preferably slightly longer than lead wires 33 and 34. When the lead wires are loaded in the grooves as heretofore described, the end of the lead wire 32 is projected out further than the ends of the lead wires 33 and 34, and then is bent at a right angle in a horizontal plane, substantially as illustrated in FIGURE 8. Next, the ends of the three lead wires 32—34 are subjected to a press having a die which bends the end of the center lead wire 33 down to the same plane as leads 32 and 34 and simultaneously flattens the ends 32a—34a preparatory to receiving a transistor wafer and the very fine whisker wires. Any other required lead positioning or shape can be accommodated so long as a mold parting line can be established, as well as different numbers of lead wires. A transistor wafer 39 is then alloyed to the flattened end 32a using gold foil as heretofore described, and whisker wires 40 connected between the expanded base contact of the transistor wafer and the flattened end 33a, and wire 41 is connected between the expanded emitter contact of the transistor wafer and the flattened end 34a substantially as shown in FIGURE 10. The cantilevered ends of the lead wires 32—34 are then inserted in a transfer mold and the ends of the lead wires, the transistor wafer and the lead wires 39, 40 and 41 encapsulated in a plastic body 42 substantially as shown in FIGURE 11. The transistor may then be tested while still in the carrier block 30, and when the test has been completed, may be removed from the carrier block 30 by pulling on the body 42 so as to move the lead wires longitudinally from the grooves 36—38. The resulting transistor is illustrated in FIGURE 12, although again the plastic body 42 is opaque rather than clear as shown in the drawing.

Each of the carrier blocks 10 is fabricated as illustrated in FIGURES 13—15. The carrier block 10 is generally rectangular in shape and has generally flat upper and lower surfaces 50 and 52 (Figures 14 and 15), generally flat side surfaces 54 and 56 (Figure 13), and generally flat end surfaces 58 and 60 (Figure 13). A retaining groove 62 is formed in the lower face 52 and extends transversely of the carrier block 10, which is preferably symmetrical about the groove 62 so as to prolong the useful life of the block. The grooves 16—18 are formed in the upper surface 50 and extend parallel over the entire length of the block between both end surfaces 58 and 60 and opening onto said end surfaces 58 and 60. It will be noted that the bottoms of the grooves are oriented in a common plane. Two alignment grooves 64 are formed in each of the side surfaces 54 and 56, one on each side of the retainer groove 62, and extend upwardly from the bottom surface 52, preferably to the top surface 50. The alignment grooves 64 are generally semicircular in cross section, but are slightly less than semicircular, so that an alignment pin forced between two adjacent blocks will separate the blocks slightly.

As can be seen in FIGURE 15, each of the grooves 16—18 is enlarged at the upper ends 16a—18a, respectively, to facilitate forcing the lead wires 12—14 into the respective grooves. The lower portions of the grooves 16—18 preferably have parallel sides which are spaced apart a distance less than the diameter of the leads 12—14 so that the leads will be retained in the grooves by a tight friction fit.

The carrier block 30 used in the process illustrated in FIGURES 8—11 may have the identical plan view and side view illustrated in FIGURES 13 and 14, but an end view as illustrated in FIGURE 16. It will be noted from FIGURE 16 that the center groove 37 is oriented at a higher position than the two outer grooves 36 and 38, as previously described in connection with the process of FIGURES 8—11.

A tray constructed for carrying twenty of the carrier blocks 10 is indicated generally by the reference numeral 80 in FIGURES 17—19. The tray 80 is comprised essentially of a length of aluminum extrusion 82 having a cross-section configuration substantially as illustrated in FIGURE 18. The extrusion 82 has a base plate 84 having front and rear edges 87 and 88, an upper plate 90 which is connected to a web 86 extending upwardly from the base plate 84 adjacent the rear edge 88. The upper plate 90 has a forwardly extending portion 92 which extends over a portion of the base plate 84, and a rearwardly extending portion 94 which may be provided with serrations 96 and 98 on the upper and lower surfaces to facilitate grasping the flange with the fingers.

The base plate 84 has a retainer rib 100 extending longitudinally of the flange which is adapted to be received in the retainer groove 62 of the carrier blocks 10 illustrated in dotted outline in FIGURE 18, or of course carrier blocks 30. The web 86 is located sufficiently rearwardly of the rib 100 as to clear the rear end of the carrier blocks 10, and the forwardly extending flange portion 92 of the upper plate extends over the end of the carrier block 10 so as to retain the carrier blocks 10 in position on the rib 100. The rib 100 and the location of the flange 92 and the web portion 86 are such as to permit very free sliding and a wobbling movement of the carrier blocks 10.

The web portion 86 includes a dovetailed channel 102 which is adapted to closely re-

ceive the enlarged root sections 104 of a pair of leaf springs 106 (Figure 17). The remainder of the leaf springs 106 are sufficiently narrow to freely pass from the dovetailed groove 102. The ends of the springs 106, as best seen in FIGURE 17, provide tips 108 which project beyond the forward face of the web section 86 and engage the rear ends of the carrier blocks 10 to prevent the carrier blocks from sliding out the ends of the retaining chamber formed by rib 100, base plate 84 and top plate 92. The root sections 104 are retained in the dovetail grooves by the stakes 110. When the spring 106 is pulled back as illustrated at the left hand end of the tray 80 in FIGURE 17, the carrier blocks 10 can be loaded into or emptied from the tray.

When twenty carrier blocks are positioned between the tips 108 of the two springs 106 in the tray illustrated, there is still a slight spacing between each adjacent pair of carrier blocks 10. Twenty-one guide holes 112 are drilled at equally spaced positions through the base plate 84 forward of the rib 100 at intervals to be aligned with the bores formed by the alignment grooves 64 between each adjacent pair of carrier blocks 10. As mentioned, each of the alignment grooves 64 is slightly less than a full semicircle, but has the same radius of curvature as the holes 112. At each station where an operation is to be performed on the ends of the lead wires 12—14, alignment pins 114 (Figure 18) are passed through one or more of the guide holes 112 and between the adjacent pairs of carrier blocks 10. When a pin 114 is inserted through each hole 112, each of the carrier blocks is precisely located and all losseness of the carrier blocks is substantially eliminated. This permits precision operations to be carried out on the cantilevered ends of the leads 12—14 which are then located at precisely predetermined positions. Varying degrees of alignment can also be obtained by eliminating certain of the pins 114 where some movement of the cantilevered leads is desired.

In the process illustrated in FIGURES 1—5, the tray 80 is customarily placed on a series of twenty-one pins so that the ends of each set of lead wires will be precisely oriented with respect to that station and will be held very steady. In carrying out the step illustrated in FIGURE 1, the leads 12—14 are customarily loaded into all of the carrier blocks 10 at the same time using a single vacuum pickup head. Then the tray is inserted in a press, using all of the guide pins, and all of the leads simultaneously forced into the bottoms of the respective grooves 16—18. The tray 80 is then moved to a press where it is positioned on a new set of guide pins and the flattened ends 12a—14a of the leads of all twenty carrier blocks simultaneously formed. The square of gold foil 20 is then placed on the flattened ends 13a, one at a time, by hand. Generally no indexing is required for this step, although the cantilevered ends of the leads are placed on a heated surface to melt the gold foil 20. Next, the tray 80 is placed on a machine having an indexing carriage without alignment pins for each of the holes 112, and the carrier blocks are successively indexed past a heating station, including microscope, where the semiconductor wafers 22 are successively placed on the spots of gold metal 20 by hand or other means and the wafers 22 alloyed to the flattened ends 13a. Next, the tray 80 is placed on the indexing carriage of a ball bonding machine, which may also include all twenty-one guide pins, and the carrier blocks successively indexed past the ball bonding station so that the whisker wire leads 24 and 26 may be bonded in position. Finally, the trays 80 and the twenty carrier blocks are taken to a transfer mold which will now be described.

A transfer molding apparatus is indicated generally by the reference numeral 120 in FIGURES 20 and 21. The molding apparatus is comprised of a lower mold half, indicated generally by the reference numeral 122, and an upper mold half, indicated generally by the reference numeral 124. The lower mold half 122 is shown in plan view in FIGURE 20 and includes the lower half of a single channel or runner 126 which supplies fluid plastic to a row of individual mold cavities 128 on one side, and a row of individual mold cavities 130 on the other side through gates 132 and 134, respectively. The lower mold half 122 includes support means for supporting a pair of trays 80a and 80b at the proper position so that the ends of the wires 32—34 carried by each of the twenty carrier blocks 30 in the tray will be positioned over the cavities 128 and 130, respectively. For example, the front edges of each of the trays is conveniently supported by a series of pedestals threaded into the body of the lower mold half which have smaller alignment pins 114a and 114b located to extend through every fourth alignment hole 112 of the respective trays 80a and 80b. The rear edges of the trays are supported by the heads of screws 136 and 138, as best seen in FIGURE 21.

The lower mold half 122 includes guide inserts 140a and 140b which contain a series of V slots for receiving and precisely positioning each of the lead wires extending from each of the carrier blocks 30 in the appropriate semicircular slots formed in the edges of sealing inserts 142a and 142b. The sealing inserts 142a and 142b mate with similar sealing inserts 144a and 144b in the upper mold half 124 to form a seal around each of the lead wires and form the ends of the mold cavities. It will be noted that when alignment

pins 114a and 114b are positioned only in every fourth hole, there remains some play between the carrier blocks 30 so as to permit the V-grooves of the guide inserts 140a and 140b to precisely position the wires in the proper slots of the sealing inserts 142a and 142b. The side walls of the cavities 128 and 130 are formed by inserts 146a and 146b, and the other end walls of the cavities, the lower half of the runner channel 126 and the lower halves of the gates 132 and 134 are formed by a center insert 150. The upper mold half 124 also has guide inserts 152a and 152b which mate with inserts 140a and 140b, the sealing inserts 144a and 144b previously mentioned which mate with the sealing inserts 142a and 142b, inserts 154a and 154b which form the upper halves of the side walls of the individual mold cavities 128 and 130, and an insert 156 which forms the upper half of the runner channel 126 and the gates 132 and 134.

Rods 158a and 158b extend upwardly through the lower mold half 122 into the cavities 128 and 130, respectively, and rod 160 extends into the runner channel 126 to force the molded bodies from the lower mold half, and rods 162a and 162b extend downwardly through the upper mold half 124 to the cavities 128 and 130, and rod 164 extends downwardly to the runner channel 126 to force the molded parts from the upper mold half.

The fluid plastic material is introduced to each of the individual mold cavities, substantially as illustrated in FIGURE 22. Thus, the gate 134 is positioned below the ends of the lead wires and is directed substantially parallel to the whisker wires 40 and 41 so that the whisker wires will not be broken by the relatively high velocity incoming fluid. In this connection, when encapsulating the devices illustrated in FIGURE 5, the gates are oriented at the sides of the individual cavities, rather than at the ends as illustrated in FIGURE 20, so that the fluid plastic will still be introduced parallel to the very fine whisker wires 24 and 26.

Thus, in the operation of the molding apparatus 120, two trays 80a and 80b, each loaded with twenty carrier blocks 30 which each carry a transistor at the stage of fabrication illustrated in FIGURE 10, are placed over the alignment pins 114a and 114b on the lower mold half 122. The V-grooves in the alignment inserts 140a and 140b precisely position each lead wire in the appropriate groove formed in the sealing inserts 142a and 142b. The mold halves are continuously heated to the necessary curing temperature for the plastic. Then the upper mold half 124 is lowered to seal the individual cavities 128 and 130. Hot thermosetting plastic is then forced under pressure, at relatively high velocity, through the channel 126. The fluid plastic flows to the end of the channel 126 and then sequentially fills the cavities 128 and 130. The cavities are filled in less than fifteen seconds, then allowed to cure for about thirty seconds to ensure that the plastic is hardened. The individual cavities 128 and 130, the gates 132 and 134 and the runner channel 126 are then all filled with cured plastic.

As the upper mold 124 is raised, rods 162a, 162b and 164 remain in position so as to push the molded bodies from the upper mold half. Additional lift rods simultaneously raise the trays and the blocks contained therein to prevent bending the leads during ejection from mold cavities. After the upper mold half 124 has cleared, rods 158a, 158b and 160 then punch the molded bodies from the lower mold half 122. At this time, the individual transistors may be readily separated from the gates 132 and 134 without removing them from the carrier blocks 30, and the individual transistors may be electrically tested prior to removal from the carrier blocks as previously mentioned.

Another embodiment of the process of the present invention is illustrated in FIGURES 23—26. In this process, the lead wires 200 are cut to the proper lengths and one end deformed to form a locking key. For example, the end may be flattened by the same shear that cuts the wires into the desired lengths so as to form a spring 202 having first and second portions 202a and 202b which extend beyond the diameter of the wire 200 as can best be seen in FIGURE 24. Three of the wires are then inserted through bores 204 in a carrier block 206.

The carrier block 206 has grooves 208 and 210 in the top and bottom surfaces which may be used to secure the carrier block in a tray similar to the tray 80. However, such a tray would leave the rear end 212 of the carrier block 206 open so that the lead wires 200 could be inserted into the bores 204 from the rear surface. A groove 214 is formed in the rear surface 212 and intersects the bores 204. The walls of the groove 214 are dimensioned so that the projections 202a and 202b of the spring section 202 will engage the walls of the groove 214 and frictionally secure the lead wire 200 in place within the bore through the carrier block, and prevent rotation of the wire.

The ends 200a of the lead wires 200 are then processed by flattening, alloying the wafer to one lead and interconnecting the other leads and the wafer, and encapsulating as heretofore described in connection with FIGURES 1—6, or FIGURES 8—11. The solid plastic body 216 may then be pushed back against the front end of the carrier block 206 so as to push the key sections 202 from the groove 214, substantially as illustrated in FIGURE 26. The key sections 202

may then be clipped from the lead wires 200 to remove the completed transistor from the carrier block. This process has the disadvantage of resulting in the loss of a small amount of the lead wires.

From the above detailed description of preferred embodiments of the invention, it will be noted that an improved process for fabricating plastic encapsulated transistors and other semiconductor devices has been described, together with certain novel apparatus for carrying out the process, and a novel product. In the preferred forms of the process, 100% of the lead wire material is utilized. Further a much higher percentage of the plastic is utilized, typically 52% as compared with about 18%, because of the fact that a single runner 126 supplies plastic to at least twice as many cavities 128 and 130. The wires are no longer welded to tabs, and the excess lead wires need not be clipped off at the plastic body and coated with an insulating material. The individual carrier blocks may be used repeatedly, and are initially fairly inexpensive since they can be molded from plastic. The final transistor is superior because the ends of the lead wires are not near the surface of the plastic encapsulation material and because the lead wires are protected throughout the processing by the carrier blocks and are therefore straight.

Although the embodiment of the invention herein described relates to the fabrication of transistors, it is to be understood that the process is also applicable to the fabrication of many other types of semiconductor devices having a fewer or greater number of leads. When utilizing a greater number of leads, one or more devices may be connected to one or more leads and to the various leads. Then all of the devices and leads may be encapsulated in a common body of plastic.

Although preferred embodiments of the invention have been described in detail, it is to be understood that various changes, substitutions and alterations can be made therein without departing from the scope of the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. A semiconductor device consisting of a plurality of lead wires forming all the connections to the device, the lead wires being side by side and substantially parallel for the greater part of their lengths, one end of at least one of the lead wires being flattened, a semiconductor wafer bonded to the flattened end of one of the lead wires, a wire bonded to the end nearest the semiconductor wafer of each of the other lead wires and to a contact on the semiconductor wafer, and a one-piece body of thermosetting plastics material encapsulating the connected ends of the lead wires, the semiconductor wafer, and the wires interconnecting the wafer and the ends of the lead wires, the connected ends of the lead wires terminating within the body of thermosetting plastics.

2. A device according to claim 1, wherein the lead wires lie substantially in the same plane.

3. A device according to claim 1, wherein there are three lead wires lying at the apexes of a triangle.

4. A device according to claim 2, wherein said leads and said flattened ends are arranged substantially in a common plane.

5. A device according to claim 3, wherein said flattened ends and at least two of said leads are arranged in a common plane.

6. A device according to any preceding claim, wherein the flattened end of at least one lead wire extends in the direction of that lead wire.

7. A device according to any preceding claim, wherein the flattened end of said one of the lead wires to which said semiconductor wafer is bonded is the flattened end extending in the direction of said lead wire.

8. A device according to any of claims 1 to 6, wherein the flattened end of said one of said lead wires to which said semiconductor wafer is bonded is arranged substantially perpendicular to the length of the respective lead wire.

9. A device according to any preceding claim, wherein all of said lead wires have flattened ends arranged in a common plane.

10. A device according to claim 9, wherein said plastics body has a flat portion substantially parallel to said common plane.

11. A device according to any preceding claim, wherein the or each flattened portion is of a different cross-section from its associated lead wire.

12. A semiconductor device substantially as herein described with reference to Figure 7 or Figure 12 of the accompanying drawings.

13. A process for encapsulating a semiconductor device, comprising the steps of:

frictionally securing substantially parallel portions of a plurality of lead wires side by side in a carrier block with one end of each lead wire cantilevered out from the carrier block, one cantilevered end of a lead wire being flattened,

mounting a semiconductor wafer on the flattened end and electrically connecting the wafer to the cantilevered ends of the other lead wires, encapsulating the cantilevered ends of the lead wires, the wafer and the electrical connections in a one-piece body of plastics material to seal the wafer in a stabilizing environment and mechanically rigidify the device, and

removing the lead wires from the carrier block.

14. A process according to claim 13, wherein the lead wires are each frictionally

may then be clipped from the lead wires 200 to remove the completed transistor from the carrier block. This process has the disadvantage of resulting in the loss of a small amount of the lead wires.

From the above detailed description of preferred embodiments of the invention, it will be noted that an improved process for fabricating plastic encapsulated transistors and other semiconductor devices has been described, together with certain novel apparatus for carrying out the process, and a novel product. In the preferred forms of the process, 100% of the lead wire material is utilized. Further a much higher percentage of the plastic is utilized, typically 52% as compared with about 18%, because of the fact that a single runner 126 supplies plastic to at least twice as many cavities 128 and 130. The wires are no longer welded to tabs, and the excess lead wires need not be clipped off at the plastic body and coated with an insulating material. The individual carrier blocks may be used repeatedly, and are initially fairly inexpensive since they can be molded from plastic. The final transistor is superior because the ends of the lead wires are not near the surface of the plastic encapsulation material and because the lead wires are protected throughout the processing by the carrier blocks and are therefore straight.

Although the embodiment of the invention herein described relates to the fabrication of transistors, it is to be understood that the process is also applicable to the fabrication of many other types of semiconductor devices having a fewer or greater number of leads. When utilizing a greater number of leads, one or more devices may be connected to one or more leads and to the various leads. Then all of the devices and leads may be encapsulated in a common body of plastic.

Although preferred embodiments of the invention have been described in detail, it is to be understood that various changes, substitutions and alterations can be made therein without departing from the scope of the invention as defined by the appended claims.

WHAT WE CLAIM IS:—

1. A semiconductor device consisting of a plurality of lead wires forming all the connections to the device, the lead wires being side by side and substantially parallel for the greater part of their lengths, one end of at least one of the lead wires being flattened, a semiconductor wafer bonded to the flattened end of one of the lead wires, a wire bonded to the end nearest the semiconductor wafer of each of the other lead wires and to a contact on the semiconductor wafer, and a one-piece body of thermosetting plastics material encapsulating the connected ends of the lead wires, the semiconductor wafer, and the wires interconnecting the wafer and the ends of the lead wires, the connected ends of the lead wires terminating within the body of thermosetting plastics.

2. A device according to claim 1, wherein the lead wires lie substantially in the same plane.

3. A device according to claim 1, wherein there are three lead wires lying at the apexes of a triangle.

4. A device according to claim 2, wherein said leads and said flattened ends are arranged substantially in a common plane.

5. A device according to claim 3, wherein said flattened ends and at least two of said leads are arranged in a common plane.

6. A device according to any preceding claim, wherein the flattened end of at least one lead wire extends in the direction of that lead wire.

7. A device according to any preceding claim, wherein the flattened end of said one of the lead wires to which said semiconductor wafer is bonded is the flattened end extending in the direction of said lead wire.

8. A device according to any of claims 1 to 6, wherein the flattened end of said one of said lead wires to which said semiconductor wafer is bonded is arranged substantially perpendicular to the length of the respective lead wire.

9. A device according to any preceding claim, wherein all of said lead wires have flattened ends arranged in a common plane.

10. A device according to claim 9, wherein said plastics body has a flat portion substantially parallel to said common plane.

11. A device according to any preceding claim, wherein the or each flattened portion is of a different cross-section from its associated lead wire.

12. A semiconductor device substantially as herein described with reference to Figure 7 or Figure 12 of the accompanying drawings.

13. A process for encapsulating a semiconductor device, comprising the steps of:

frictionally securing substantially parallel portions of a plurality of lead wires side by side in a carrier block with one end of each lead wire cantilevered out from the carrier block, one cantilevered end of a lead wire being flattened,

mounting a semiconductor wafer on the flattened end and electrically connecting the wafer to the cantilevered ends of the other lead wires, encapsulating the cantilevered ends of the lead wires, the wafer and the electrical connections in a one-piece body of plastics material to seal the wafer in a stabilizing environment and mechanically rigidify the device, and

removing the lead wires from the carrier block.

14. A process according to claim 13, wherein the lead wires are each frictionally

secured in a groove formed in the carrier block.

15. A process according to claim 14, wherein the lead wires are frictionally secured in a plurality of parallel grooves formed in the top surface of the carrier block.

16. A process according to claim 15, wherein the lead wires when secured in the carrier block lie in substantially the same plane.

17. A process according to claim 15, wherein there are three lead wires and when secured in the carrier block the centre lead wire is disposed above the two outer lead wires.

18. A process according to claim 13, wherein the lead wires are each frictionally secured in a bore extending through the carrier block.

19. A process according to claim 18, wherein each of the lead wires is partially deformed to form a key portion, and the carrier block is adapted to frictionally engage and retain the key portion of each lead wire.

20. A process according to claim 19, wherein the key portion is formed by flattening the end of each lead wire remote from the cantilevered end, one end of each bore is conformed to frictionally engage the flattened end, each lead wire is inserted in the bores by passing the cantilevered end of the lead wire through the conformed end of the bore until the flattened end is secured in the conformed end with the cantilevered end projecting from the carrier block by pushing the lead wires back through the bores, cutting the flattened ends from the lead wires, and then pulling the lead wires through the bores.

21. A process according to claim 13, further characterized by flattening the cantilevered ends of the lead wires, alloying a semiconductor wafer to one of the flattened cantilevered ends, and electrically interconnecting the wafer and each of the other flattened ends with ball bonded lead wires prior to encapsulation.

22. A process according to claim 13, wherein the plastics material is a thermosetting plastic and is moulded by a transfer moulding process.

23. A process for encapsulating plastics encapsulated semiconductor devices according to any of claims 13 to 22, including the steps of locating a plurality of carrier block assemblies each having a plurality of lead wires cantilevered therefrom with a semiconductor wafer mounted on one of the cantilevered ends and electrically connected to the other cantilevered ends of the lead wires in that carrier block, the carrier blocks being disposed in side-by-side relationship in two parallel rows with the cantilevered lead wires of each of the blocks in each row extending toward the other row and into an individual mould cavity, the individual mould cavities being arranged in two adjacent rows, and introducing a fluid thermosetting plastic into each of the mould cavities from a single supply passageway extending between the two rows of mould cavities.

24. A process according to claim 14, wherein the carrier block comprises a body of resilient material having a plurality of grooves formed in one surface for receiving the said lead wires, each of the grooves having a depth greater than one-half the diameter of the lead wire to be retained therein and a width less than the diameter of the lead wire whereby a lead wire can be pressed into each of the grooves and frictionally retained in the respective grooves with the ends of the lead wires cantilevered out from the carrier block.

25. A process as defined in claim 24, wherein the grooves are formed in one surface of the body, the bottoms of the grooves lie in a common plane, and the bottoms of the grooves extend to an opening at another surface of the body.

26. A process as defined in claim 24, wherein there are three grooves formed in one surface of the body, and the bottoms of the grooves are straight and substantially parallel and lie at the corners of a triangle.

27. A process as defined in claim 24, wherein the body is generally rectangular in shape having generally parallel top and bottom faces, generally parallel side faces, and generally parallel end faces, and wherein the grooves are formed in the top face and open at both end faces.

28. A process as defined in claim 27, wherein the bottoms of the grooves lie in a common plane.

29. A process as claimed in claim 27, wherein there are three grooves and the bottoms of the two centre grooves lie in the same plane and the bottom of the centre groove lies above said plane.

30. A process as defined in claim 27, wherein the carrier block also includes a groove extending transversely across at least one of the top and bottom surfaces for mounting the carrier block in a tray.

31. A process as defined in claim 27, wherein the carrier block also includes an alignment groove in each of the side faces extending to the bottom surface, the grooves in the two side faces being aligned such that the alignment grooves of two carrier blocks disposed in side-by-side relationship will form a single passageway for receiving a common alignment pin.

32. A process according to claim 23, wherein each carrier block assembly is generally rectangular and has top and bot-

tom surfaces, opposite side surfaces and front and rear end surfaces with a plurality of grooves formed in the top surface and extending to the front end surface, a transverse groove in at least one of the top and bottom surfaces extending between the side surfaces, and an alignment groove extending in each of the side surfaces and extending to the bottom surface the alignment grooves being disposed one opposite the other, the carrier block assemblies being disposed in a tray comprising an elongated body having a substantially uniform cross-section characterized by a base plate for supporting the carrier blocks in side-by-side relationship extending transversely of the elongated body, a top plate extending over a portion of the top surfaces adjacent the rear end surfaces but leaving the grooves in the top surfaces exposed adjacent the front end surfaces, means extending by the rear end surface and connecting the top plate to the base plate, a rib formed on at least one of the base or top plates and adapted to enter the respective transverse grooves and retain the carrier blocks between the plates, means at each end of the tray for retaining the carrier blocks on the rib, and a plurality of alignment holes in the base plate positioned to receive alignment pins projecting upwardly through the alignment holes into the alignment grooves between adjacent pairs of carrier blocks.

33. A process according to claim 23, wherein the said two adjacent rows of mould cavities are disposed parallel to each other and are defined by a transfer mould which also includes a conduit extending between the two rows of mould cavities and in fluid communication with each of the mould cavities through a restrictive passageway for supplying a thermosetting fluid plastic under pressure to each of the cavities, and means disposed adjacent each row of cavities for supporting the carrier blocks, lead wires and semiconductor wafers in an aligned position with the cantilevered ends of the lead wires extending into the respective mould cavities.

34. A process for encapsulating a semiconductor device substantially as herein described with reference to Figures 1 to 6, Figures 8 to 11, or modified as described with reference to Figure 13, Figures 14 to 16, Figures 17 to 19, Figures 20 to 22, or Figures 23 to 26.

35. A semiconductor device encapsulated by a process according to any of claims 13 to 34.

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