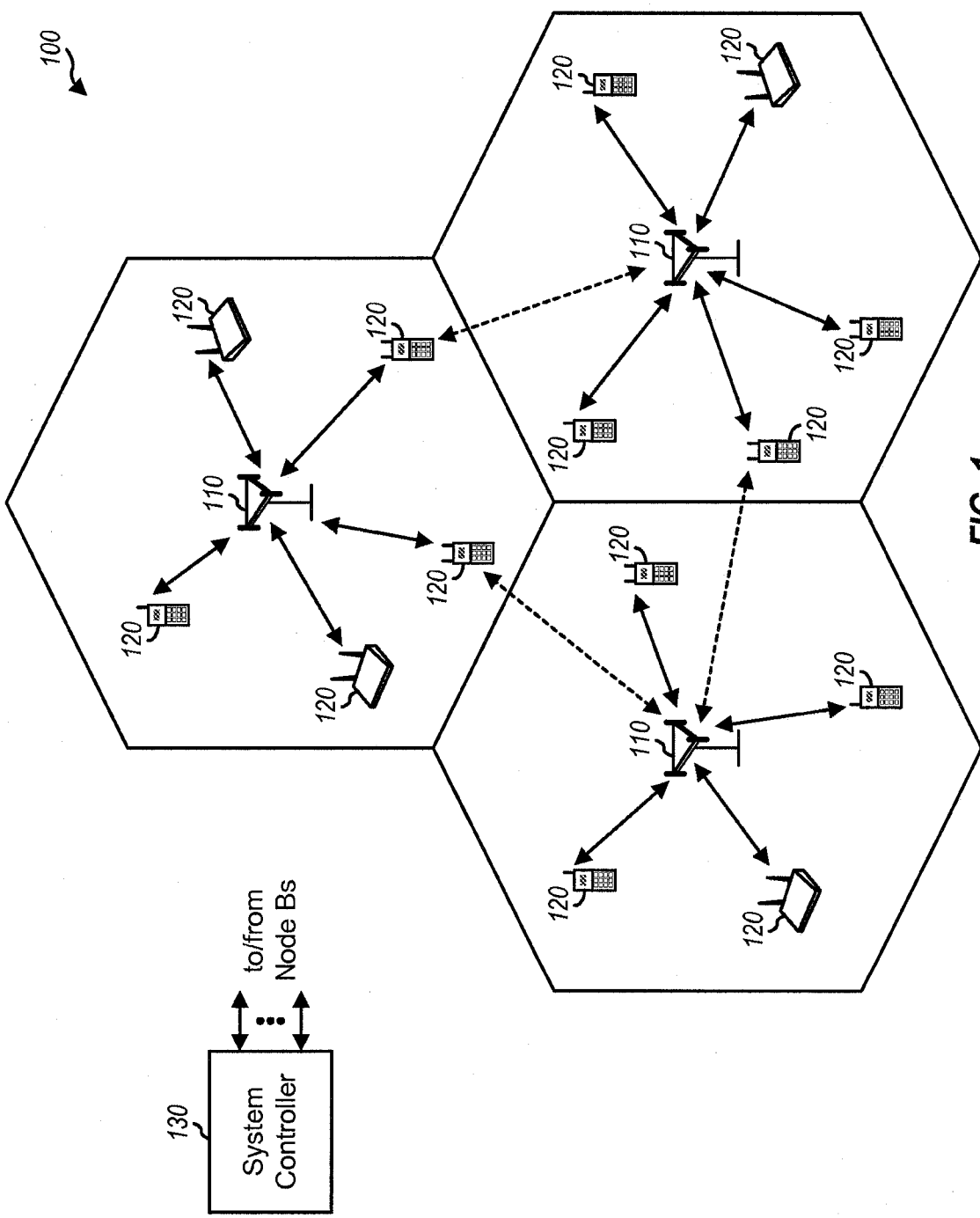


FIG. 1

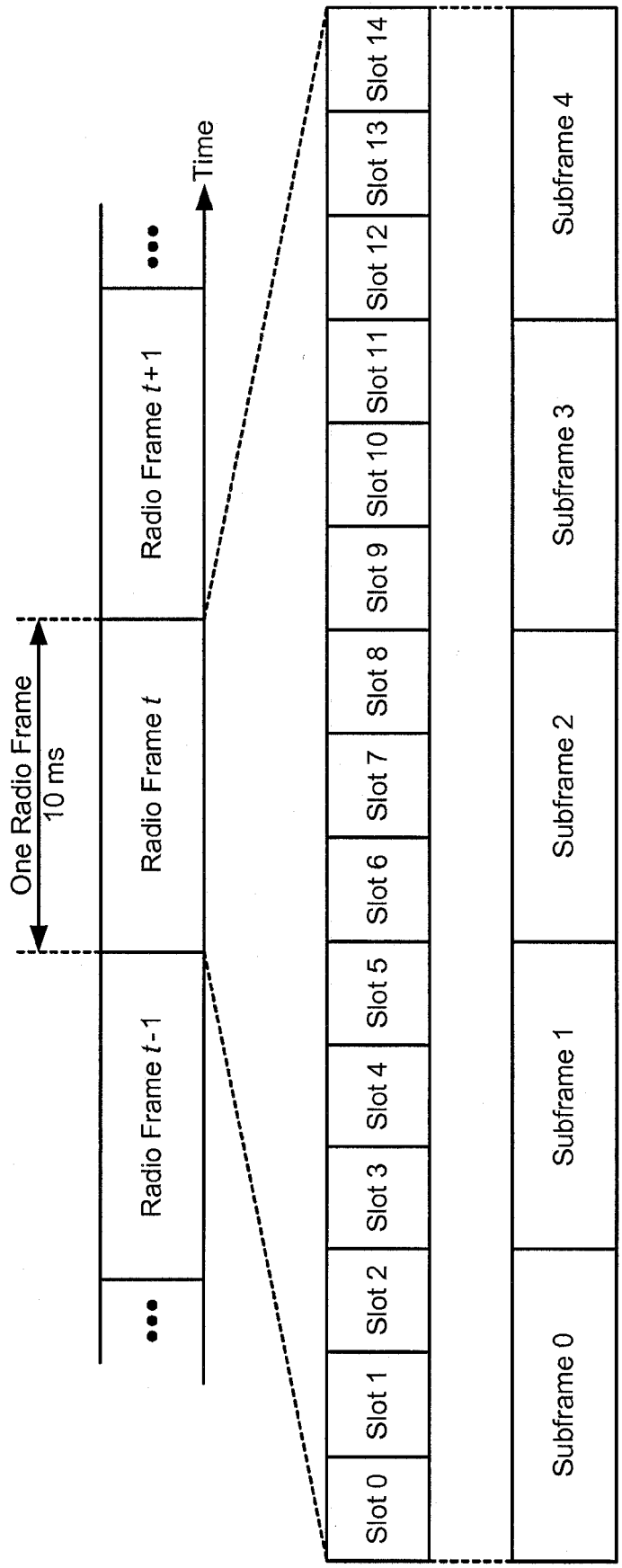

Time
One Radio Frame
10 ms
Radio Frame t-1
Radio Frame t
Radio Frame t+1
Slot 0
Slot 1
Slot 2
Slot 3
Slot 4
Slot 5
Slot 6
Slot 7
Slot 8
Slot 9
Slot 10
Slot 11
Slot 12
Slot 13
Slot 14
Subframe 0
Subframe 1
Subframe 2
Subframe 3
Subframe 4

FIG. 2

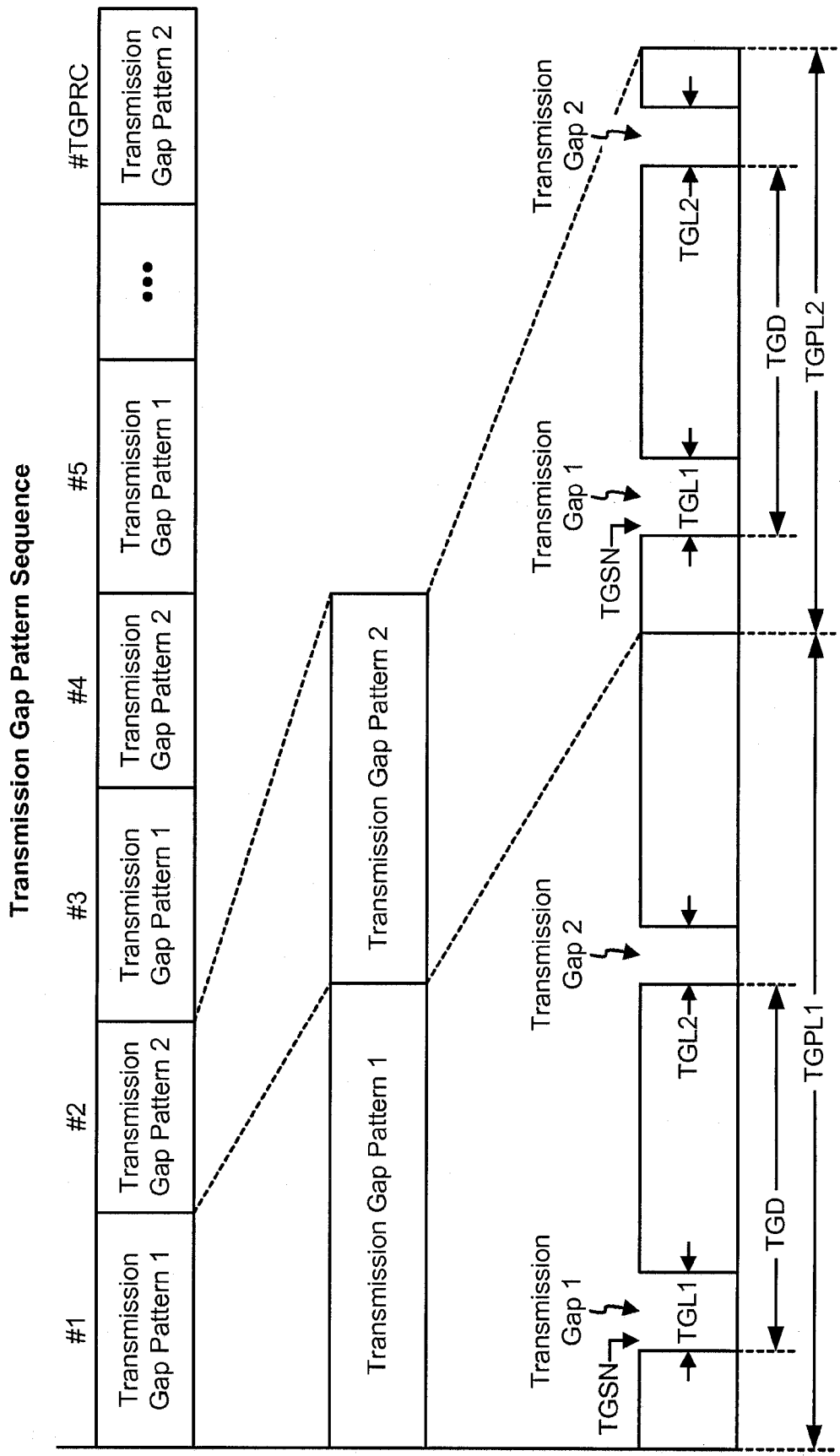

Transmission Gap Pattern Sequence
#1
#2
#3
#4
#5
#TGPRC
Transmission Gap Pattern 1
Transmission Gap Pattern 2
Transmission Gap Pattern 1
Transmission Gap Pattern 2
Transmission Gap Pattern 1
Transmission Gap Pattern 2
Transmission Gap 1
Transmission Gap 2
TGSN
TGL1
TGL2
TGD
TGPL1
TGPL2

FIG. 3

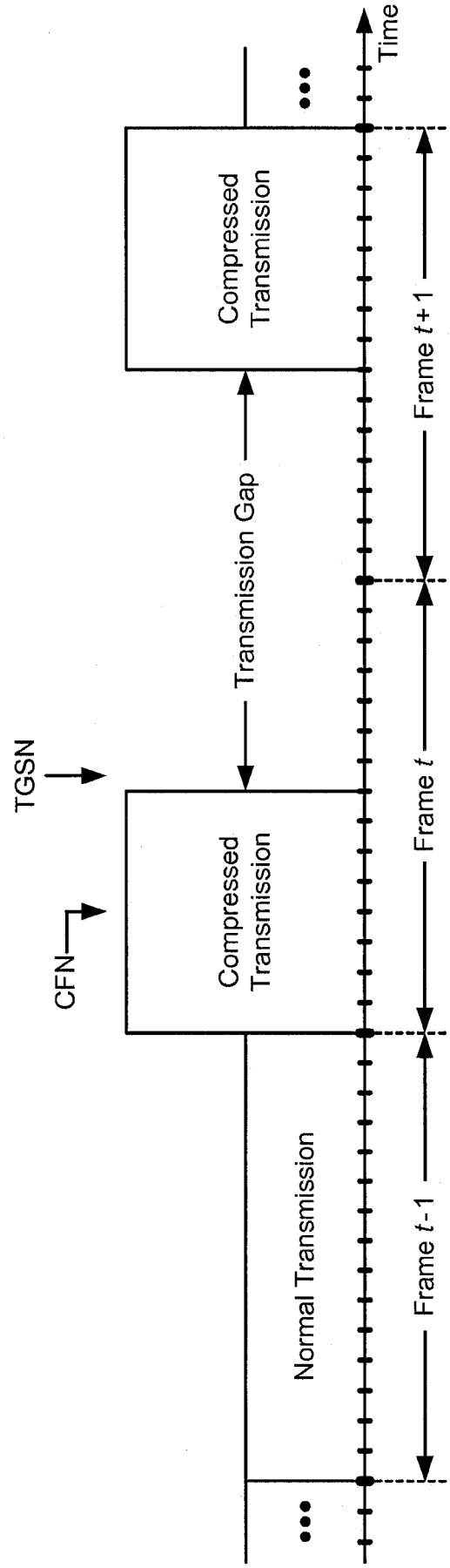

Time
Compressed Transmission
Transmission Gap
Frame t + 1
TGSN
CFN
Compressed Transmission
Frame t
Normal Transmission
Frame t - 1

FIG. 4

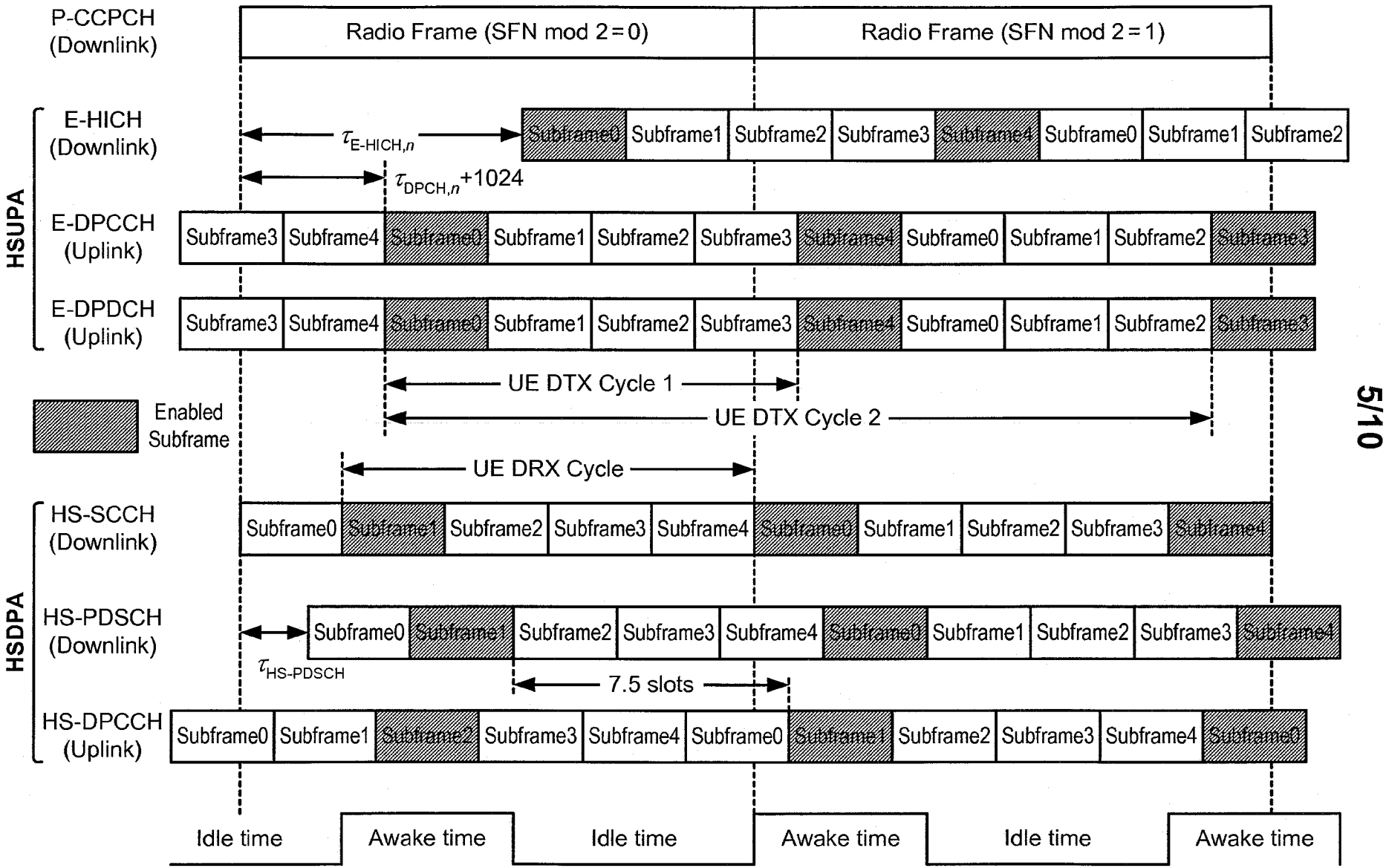

P-CCPCH (Downlink)
Radio Frame (SFN mod 2 = 0)
Radio Frame (SFN mod 2 = 1)
HSUPA
E-HICH (Downlink)
$\tau_{E\text{-}HICH,n}$
$\tau_{DPCH,n}$+1024
Subframe0 Subframe1 Subframe2 Subframe3 Subframe4 Subframe0 Subframe1 Subframe2
E-DPCCH (Uplink)
Subframe3 Subframe4 Subframe0 Subframe1 Subframe2 Subframe3 Subframe4 Subframe0 Subframe1 Subframe2 Subframe3
E-DPDCH (Uplink)
Subframe3 Subframe4 Subframe0 Subframe1 Subframe2 Subframe3 Subframe4 Subframe0 Subframe1 Subframe2 Subframe3
UE DTX Cycle 1
UE DTX Cycle 2
Enabled Subframe
UE DRX Cycle
HSDPA
HS-SCCH (Downlink)
Subframe0 Subframe1 Subframe2 Subframe3 Subframe4 Subframe0 Subframe1 Subframe2 Subframe3 Subframe4
HS-PDSCH (Downlink)
Subframe0 Subframe1 Subframe2 Subframe3 Subframe4 Subframe0 Subframe1 Subframe2 Subframe3 Subframe4
$\tau_{HS\text{-}PDSCH}$
7.5 slots
HS-DPCCH (Uplink)
Subframe0 Subframe1 Subframe2 Subframe3 Subframe4 Subframe0 Subframe1 Subframe2 Subframe3 Subframe4 Subframe0
Idle time
Awake time
Idle time
Awake time
Idle time
Awake time

FIG. 5

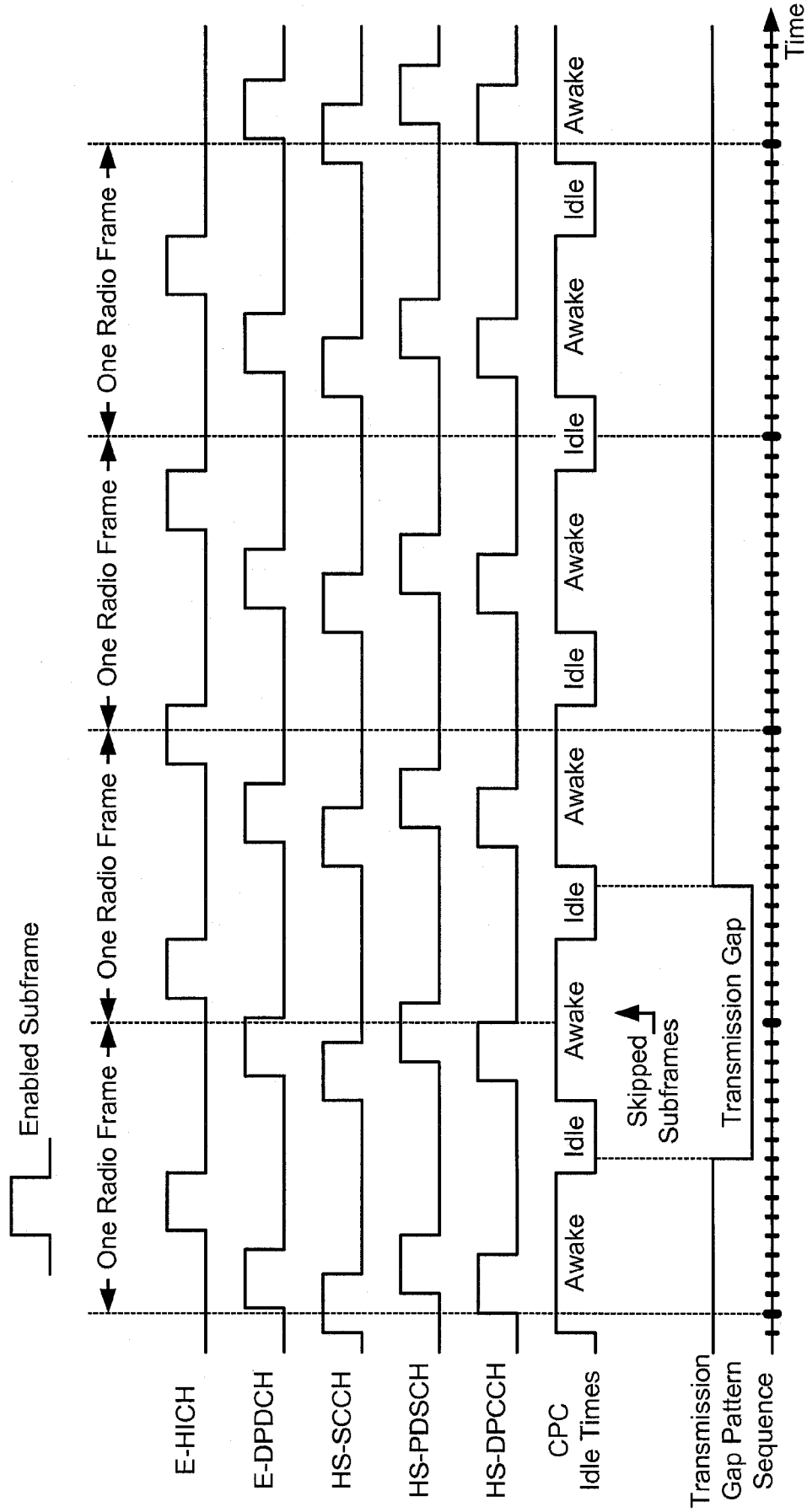

Enabled Subframe
One Radio Frame
One Radio Frame
One Radio Frame
One Radio Frame
E-HICH
E-DPDCH
HS-SCCH
HS-PDSCH
HS-DPCCH
CPC
Idle Times
Transmission
Gap Pattern
Sequence
Awake
Idle
Awake
Idle
Awake
Idle
Awake
Idle
Awake
Skipped
Subframes
Transmission Gap
Time

FIG. 6

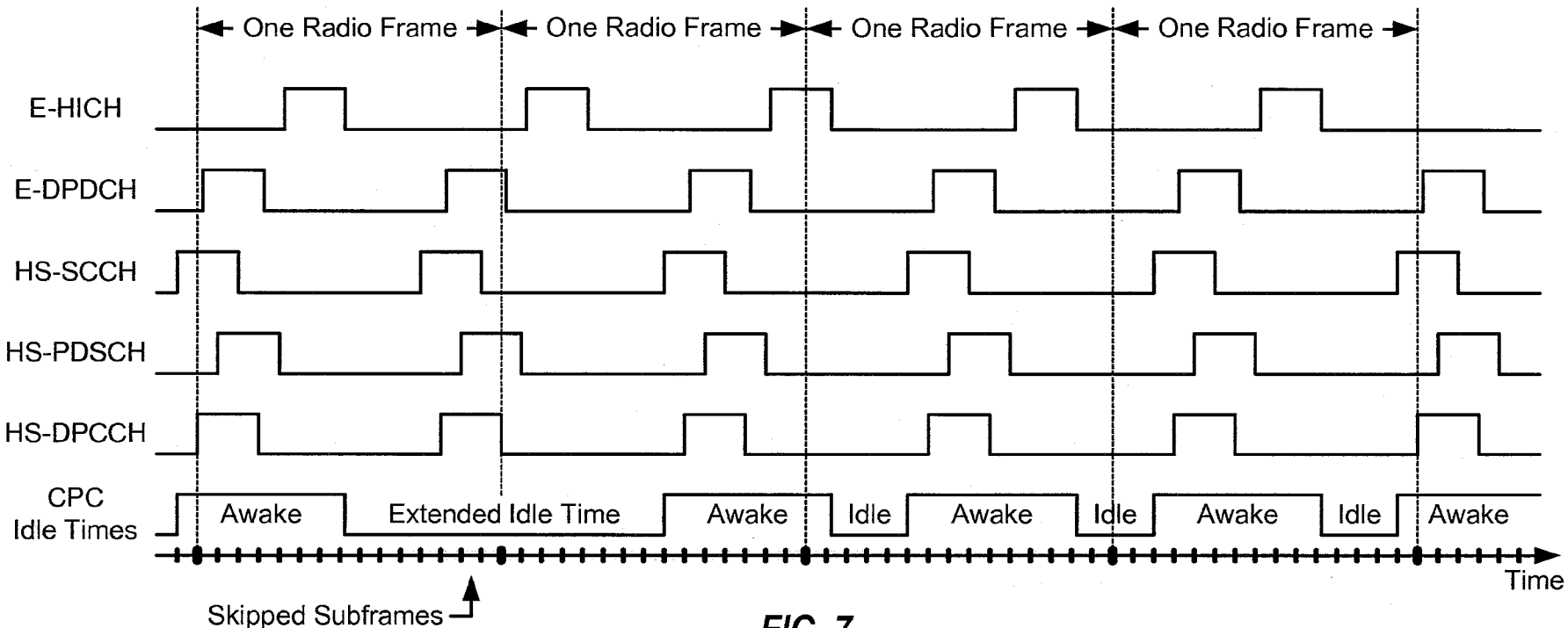


FIG. 7

800

Part 1		Part 2			
Channelization Code Set	Mod	Format ID (e.g., '111110')	Order Type (e.g., '001' = CM order)	Order (e.g., 1 bit = CM On/Off)	UE ID, CRC

FIG. 8

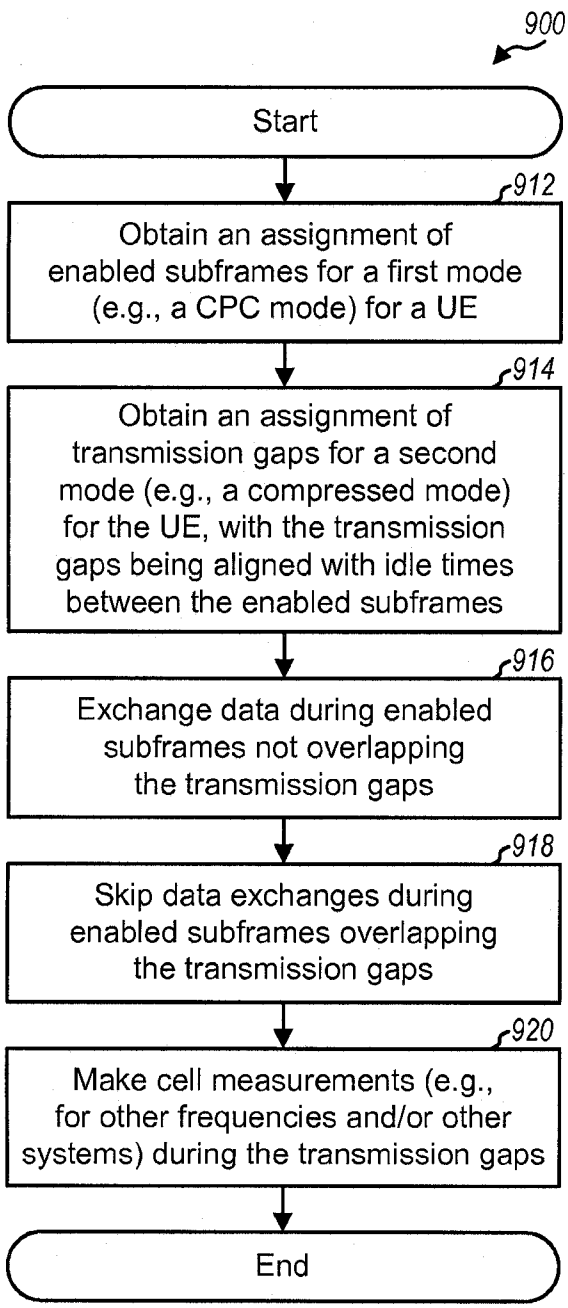

900
Start
912
Obtain an assignment of enabled subframes for a first mode (e.g., a CPC mode) for a UE
914
Obtain an assignment of transmission gaps for a second mode (e.g., a compressed mode) for the UE, with the transmission gaps being aligned with idle times between the enabled subframes
916
Exchange data during enabled subframes not overlapping the transmission gaps
918
Skip data exchanges during enabled subframes overlapping the transmission gaps
920
Make cell measurements (e.g., for other frequencies and/or other systems) during the transmission gaps
End

FIG. 9

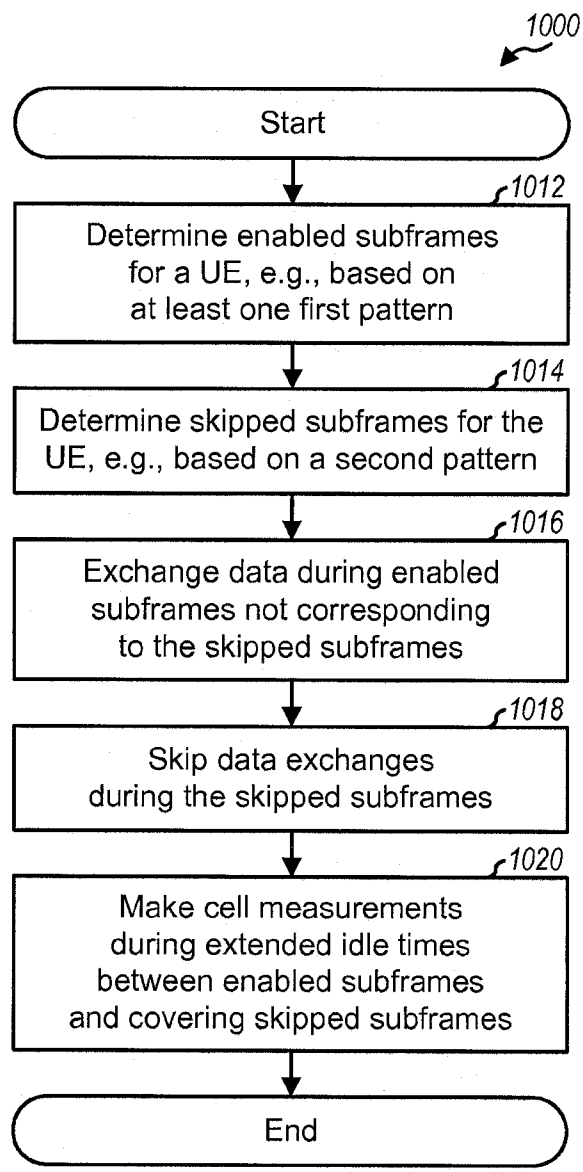

1000
Start
1012
Determine enabled subframes for a UE, e.g., based on at least one first pattern
1014
Determine skipped subframes for the UE, e.g., based on a second pattern
1016
Exchange data during enabled subframes not corresponding to the skipped subframes
1018
Skip data exchanges during the skipped subframes
1020
Make cell measurements during extended idle times between enabled subframes and covering skipped subframes
End

FIG. 10

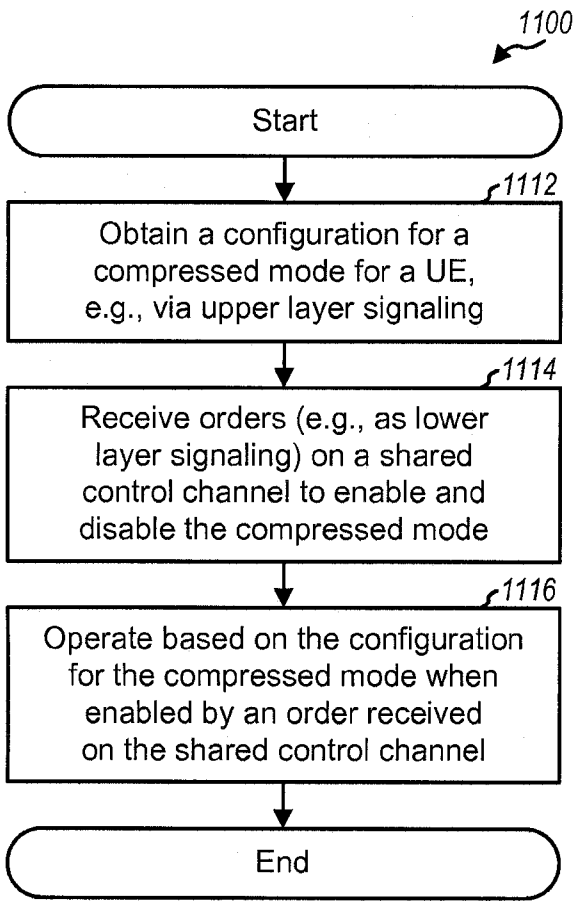

1100
Start
1112
Obtain a configuration for a compressed mode for a UE, e.g., via upper layer signaling
1114
Receive orders (e.g., as lower layer signaling) on a shared control channel to enable and disable the compressed mode
1116
Operate based on the configuration for the compressed mode when enabled by an order received on the shared control channel
End

FIG. 11

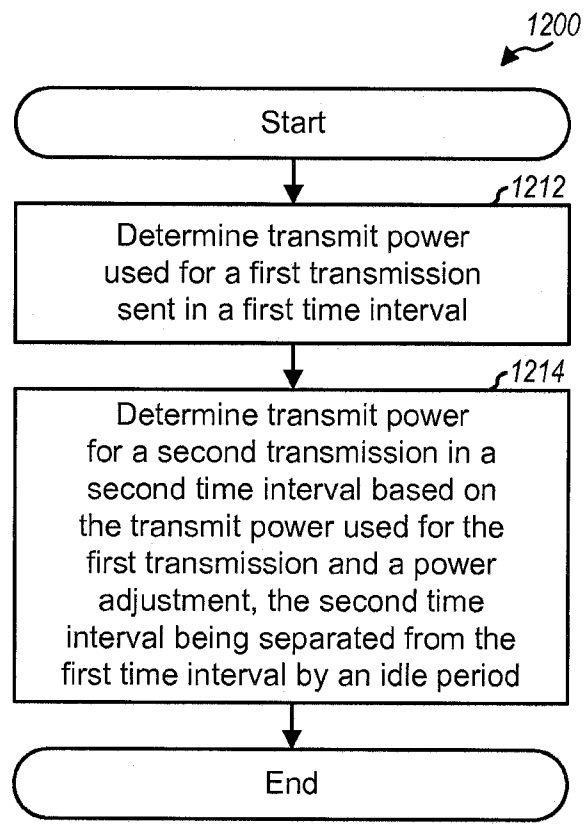

1200
Start
1212
Determine transmit power used for a first transmission sent in a first time interval
1214
Determine transmit power for a second transmission in a second time interval based on the transmit power used for the first transmission and a power adjustment, the second time interval being separated from the first time interval by an idle period
End

FIG. 12

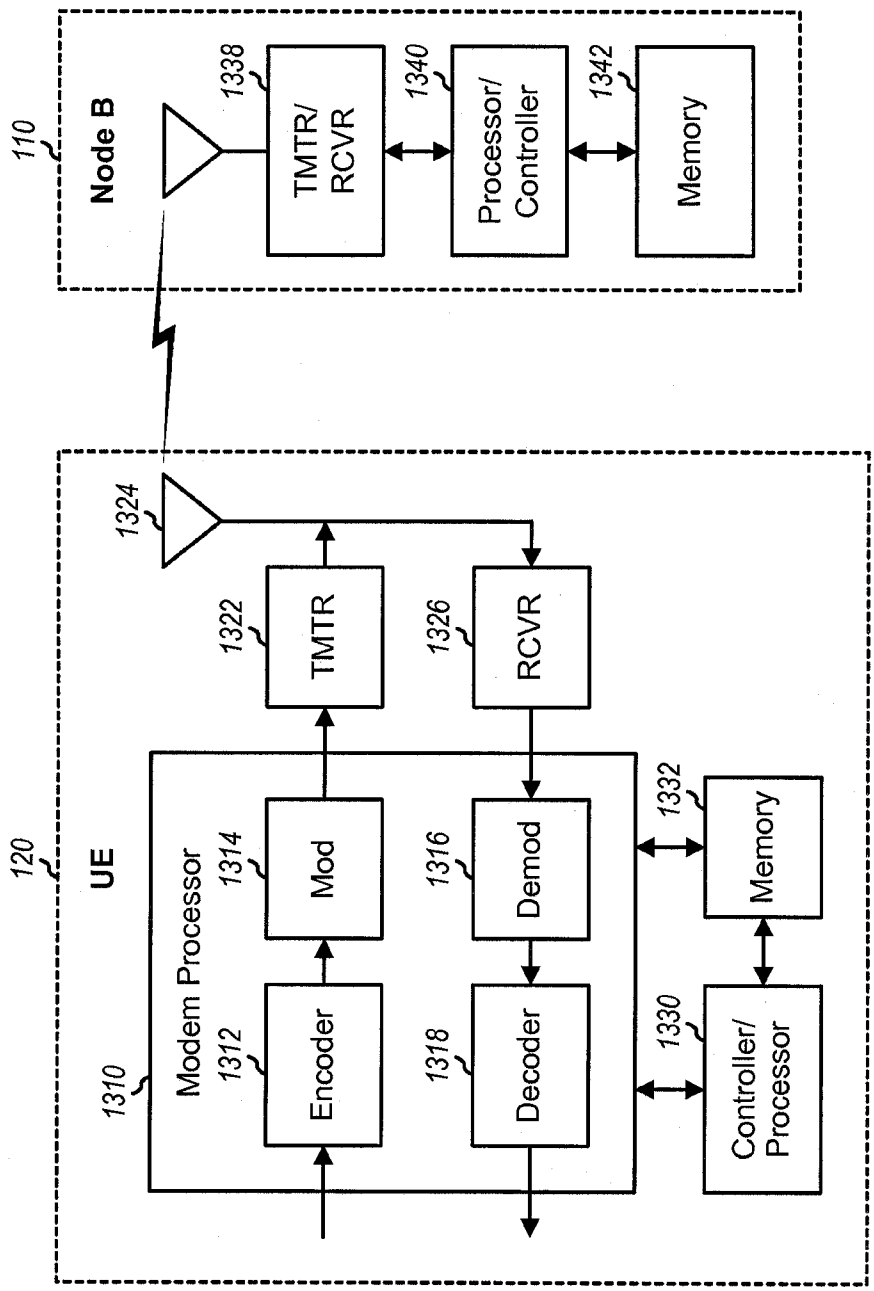

110
Node B
1338
TMTR/
RCVR
1340
Processor/
Controller
1342
Memory
120
UE
1324
1322
TMTR
1326
RCVR
1310
Modem Processor
1312
Encoder
1314
Mod
1316
Demod
1318
Decoder
1330
Controller/
Processor
1332
Memory

FIG. 13