CLAIMS

1. A method of low density parity check (LDPC) coding at a transmitting wireless communication device, the method comprising: configuring a systematic bit section and a parity bit section of a circular buffer based on a selected mother code rate selected from at least two mother code rates, wherein the at least two mother code rates comprise a reduced mother code rate that is less than a minimum mother code rate at which a maximum information block size produces a maximum codeword size of a decoder at a receiving wireless communication device, wherein the circular buffer comprises a fixed length; encoding an information block utilizing LDPC coding to produce a codeword comprising systematic bits and parity bits; inserting the systematic bits into the systematic bit section and the parity bits into the parity bit section; selecting coded bits for inclusion in a redundancy version of the codeword from the systematic bits in the systematic bit section and the parity bits in the parity bit section; and transmitting a 3rd Generation Partnership Project (3GPP) signal comprising the redundancy version of the codeword over a wireless air interface.

2. The method of claim 1, wherein configuring the systematic bit section and the parity bit section of the circular buffer further comprises: defining respective sizes of the systematic bit section and the parity bit section of the circular buffer based on the selected mother code rate.

3. The method of claim 2, wherein defining the circular buffer further comprises: defining the respective sizes of the systematic bit section and the parity bit section of the circular buffer based on an information block size of the information block.

4. The method of claim 3, wherein defining the circular buffer further comprises: setting the fixed length of the circular buffer equal to a maximum length corresponding to a maximum codeword length.

5. The method of claim 3, wherein defining the circular buffer further comprises: selecting the information block size of the information block based on an absolute minimum code rate for the codeword.

6. The method of claim 3, wherein encoding the information block utilizing LDPC coding further comprising: selecting a selected base graph from at least two base graphs for LDPC coding based on the information block size.

7. The method of claim 6, wherein each of the at least two base graphs is associated with a respective one of the at least two mother code rates.

8. The method of claim 1, wherein the redundancy version comprises an initial redundancy

version or a subsequent redundancy version.

9. The method of claim 8, wherein each of the initial redundancy version and the subsequent redundancy version comprise different sets of the coded bits.

10. An apparatus comprising a transmitting wireless communication device configured for low density parity check (LDPC) coding, comprising: a transceiver; a memory; and a processor communicatively coupled to the transceiver and the memory, the processor configured to: configure a systematic bit section and a parity bit section of a circular buffer within the memory based on a selected mother code rate selected from at least two mother code rates, wherein the at least two mother code rates comprise a reduced mother code rate that is less than a minimum mother code rate at which a maximum information block size produces a maximum codeword size of a decoder at a receiving wireless communication device, wherein the circular buffer comprises a fixed length; encode an information block utilizing LDPC coding to produce a codeword comprising systematic bits and parity bits; insert the systematic bits into the systematic bit section and the parity bits into the parity bit section; select coded bits for inclusion in a redundancy version of the codeword from the systematic bits in the systematic bit section and the parity bits in the parity bit section; and transmit a 3rd Generation Partnership Project (3GPP) signal comprising the redundancy version of the codeword over a wireless air interface via the transceiver.

11. The apparatus of claim 10, wherein the processor is further configured to: define respective sizes of the systematic bit section and the parity bit section based on the selected mother code rate.

12. The apparatus of claim 11, wherein the processor is further configured to: define the respective sizes of the systematic bit section and the parity bit section of the circular buffer based on an information block size of the information block.

13. The apparatus of claim 12, wherein the processor is further configured to: setting the fixed length of the circular buffer equal to a maximum length corresponding to a maximum codeword length.

14. The apparatus of claim 12, wherein the processor is further configured to: select the information block size of the information block based on an absolute minimum code rate for the codeword.

15. The apparatus of claim 12, wherein the processor is further configured to: select a selected base graph from at least two base graphs for LDPC coding based on the information block size.

16. The apparatus of claim 15, wherein each of the at least two base graphs is associated with a respective one of the at least two mother code rates.

17. The apparatus of claim 10, wherein the redundancy version comprises an initial redundancy version or a subsequent redundancy version.

18. The apparatus of claim 17, wherein each of the initial redundancy version and the subsequent redundancy version comprise different sets of the coded bits.

19. A transmitting wireless communication device, comprising: means for configuring a systematic bit section and a parity bit section of a circular buffer based on a selected mother code rate selected from at least two mother code rates, wherein the at least two mother code rates comprise a reduced mother code rate that is less than a minimum mother code rate at which a maximum information block size produces a maximum codeword size of a decoder at a receiving wireless communication device, wherein the circular buffer comprises a fixed length; means for encoding an information block utilizing LDPC coding to produce a codeword comprising systematic bits and parity bits; means for inserting the systematic bits into the systematic bit section and the parity bits into the parity bit section; means for selecting coded bits for inclusion in a redundancy version of the codeword from the systematic bits in the systematic bit section and the parity bits in the parity bit section; and means for transmitting a 3rd Generation Partnership Project (3GPP) signal comprising the redundancy version of the codeword over a wireless air interface.

20. The wireless communication device of claim 19, wherein the means for configuring the systematic bit section and the parity bit section of the circular buffer further comprises: means for defining respective sizes of the systematic bit section and the parity bit section of the circular buffer based on the selected mother code rate.

21. The wireless communication device of claim 20, wherein the means for defining the circular buffer further comprises: means for defining the respective sizes of the systematic bit section and the parity bit section of the circular buffer based on an information block size of the information block.

22. The wireless communication device of claim 21, wherein the means for defining the circular buffer further comprises: means for setting the fixed length of the circular buffer equal to a maximum length corresponding to a maximum codeword length.

23. The wireless communication device of claim 21, wherein the means for defining the circular buffer further comprises: means for selecting the information block size of the information block based on an absolute minimum code rate for the codeword.

24. The wireless communication device of claim 21, wherein the means for encoding the information block utilizing LDPC coding further comprising: means for selecting a selected base graph from at least two base graphs for LDPC coding based on the information block size.

25. The wireless communication device of claim 24, wherein each of the at least two base graphs is associated with a respective one of the at least two mother code rates.

26. The wireless communication device of claim 19, wherein the redundancy version comprises an initial redundancy version or a subsequent redundancy version.

27. The wireless communication device of claim 26, wherein each of the initial redundancy version and the subsequent redundancy version comprise different sets of the coded bits.

28. A non-transitory computer-readable medium storing computer executable code, comprising code that when executed causes a processor within a transmitting wireless communication device to perform the steps of: configuring a systematic bit section and a parity bit section of a circular buffer based on a selected mother code rate selected from at least two mother code rates, wherein the at least two mother code rates comprise a reduced mother code rate that is less than a minimum mother code rate at which a maximum information block size produces a maximum codeword size of a decoder at a receiving wireless communication device, wherein the circular buffer comprises a fixed length; encoding an information block utilizing LDPC coding to produce a codeword comprising systematic bits and parity bits; inserting the systematic bits into the systematic bit section and the parity bits into the parity bit section; selecting coded bits for inclusion in a redundancy version of the codeword from the systematic bits in the systematic bit section and the parity bits in the parity bit section; and transmitting a 3rd Generation Partnership Project (3GPP) signal comprising the redundancy version of the codeword over a wireless air interface.

29. The non-transitory computer-readable medium of claim 28, further comprising code that when executed causes a processor to perform the step of: defining respective sizes of the systematic bit section and the parity bit section based on the selected mother code rate.

30. The non-transitory computer-readable medium of claim 29, further comprising code that when executed causes a processor to perform the step of: defining the respective sizes of the systematic bit section and the parity bit section of the circular buffer based on an information block size of the information block.