Description

Method for the production of complementary MOS transistors

The invention relates to a method for the production of complementary MOS transistors, in which each of the complementary transistors is arranged in a corresponding trough in a substrate and contains a source zone and a drain zone which each adjoin a field insulation zone and define a channel over which a gate oxide and a gate electrode are arranged.

Integrated CMOS circuits are produced by means of a multiplicity of process steps. The production costs of these circuits are determined by the process complexity and the physical processing time. Highly complex modules therefore require several hundred individual process steps to the finished product and very many days for the process cycle and the production of the product.

Integrated CMOS circuits which are produced on monocrystalline silicon wafers usually require at least seven phototechnology steps for the basic process for producing the circuit functions in the silicon and five phototechnology steps for two metallization planes together with passivation. A typical process includes a first mask for the implantation of the first trough, with respect to which the complementary trough is then implanted in a self-aligned manner and both are driven in in a following temperature step, a second mask for the production of field insulation, for example by means of local oxidation, a third mask for setting a threshold voltage of an MOS transistor, the threshold voltage of an NMOS transistor typically being effected over the whole area and the mask then being required for a PMOS transistor.

The aforementioned steps are followed by a fourth mask for gate structuring, a fifth mask for lightly doped source/drain implantation of the NMOS transistor, the so-called LDD implantation, as well as a sixth mask for

the production of the heavily doped drain of the NMOS transistor. Finally, the seventh mask is required for the implantation of the drain of the PMOS transistor.

After the production of whole-area intermediate insulation layers with contact holes by means of an eighth mask, the ninth to eleventh masks are provided for the metallization of a first layer, for the production of contact holes and for a second metallization layer. The metallization layers are usually made of aluminium. A twelfth mask is subsequently used to produce a passivation layer.

Further masks may be required in circuits which, in addition, have still further elements, for example a capacitor or a resistor. In principle, it is always desirable to have the minimum number of process steps in order to reduce the production costs and shorten the turnaround time.

The invention is based on the object of specifying a method for the production of complementary MOS transistors of the type mentioned in the introduction which requires a smaller number of process steps.

This object is achieved by means of the features of Patent Claim 1.

The invention is based on the insight that considerable complexity for the production of CMOS circuits is possible with a reduction in the number of mask steps. Although the continuing improvement in implantation equipment and the scaling of layer thicknesses make it possible to carry out the trough implantations after the production of the field insulation zones, and consequently to dispense with the time-consuming trough drive-in step, the total number of masks nevertheless remains unchanged as a result of the combination with a mask for setting the PMOS threshold voltage.

The invention provides for reducing the required number of phototechnology steps or the number of masks in the basic process for the production of the transistors from seven to four masks. This is possible by carrying

out the implantations required to realize the transistors in two successive blocks after the gate structuring, only one mask being required for each block. This means that, for the NMOS transistor, the production of the trough, of the threshold voltage of the LDD zone and of the drain zone is carried out in a block by means of succeeding implantation steps, but using only a single mask or one phototechnology step. The PMOS transistor is produced correspondingly by means of a single further phototechnology step. The essential feature here is that both implantation blocks are carried out after the gate structuring.

The thickness of the gate electrode and the energy levels of the implantation steps are coordinated with one another in such a way that the drain and the LDD implantations are reliably masked by the gate electrode. The range of the channel implantation must be greater than the thickness of the gate electrode, and the range of the trough implantation must be greater than the sum of the field oxide thickness and the thickness of the gate electrode.

For the sequence of the various implantations within a block, it is necessary to ensure that the drain implantations take place before, and the LDD implantations after, optional reduction of the spacer by isotropic etching. Implantation of heavy ions such as arsenic should be given precedence in order to avoid a knock-on effect.

The invention has the advantage that it is possible to dispense with the masks for the production of a self-aligned trough, of the PMOS threshold voltage and of the NMOS LDD zone. The only remaining photomasks for implantations are an NMOS mask and a PMOS mask. Accordingly, the overall process becomes less complex. The production costs are distinctly reduced compared with modern CMOS processes, for example by 25%. The physical processing time, too, is distinctly reduced, for example from slightly more than eleven days to less than nine days.

Refinements of the invention are characterized in subclaims.

The invention is explained in more detail below using an exemplary embodiment. In the drawings:

FIGS 1 to 4 show diagrammatic cross-sections through different stages of the production process.

In accordance with FIG 1, the process begins with the production, known per se, of field insulation zones 2 in a substrate 1. It is usual, for this purpose, first of all for a nitride layer to be applied over the whole area of the substrate and be structured by means of a first mask, which is produced using a photographic technique, and a subsequent etching step. This is followed by the production of the field insulation zones, for example in the form of field oxide. The nitride layer is subsequently removed. In addition to the conventional technology with the aid of local oxidation (LOCOS) an oxide can be chemically deposited from the vapour phase and structured, or the insulation zones are produced by anisotropic etching and filling with oxide (Shallow Trench Insulation). The arrangement according to FIG 1 is obtained.

After this, a gate oxide having a thickness typically of 15 nm is produced and a silicon layer of, for example, 200 nm is deposited. A second mask, which is produced using a second photographic technique, in conjunction with a further etching step results in a structured gate electrode 3, which is insulated from the substrate by the gate oxide 4.

The structuring of the gate electrode is typically followed by an oxidation step, by means of which an oxide layer of 10 nm is produced in the whole area. An insulation layer is conformally deposited over the latter with the aid of a CVD process (chemical deposition for example by pyrolysis of tetraethylorthosilane at reduced pressure (low-pressure CVD)) and is subsequently anisotropically etched back completely or partially with the result that at least lateral insulation webs 5 remain next to the gate electrode. Afterwards, the NMOS transis-

tors are defined using a first resist mask 6.

Deep implantation, that is to say a high implantation energy, is used to produce a retrograde p-trough 10, as is described, for example, in the book by D. Widmann et al.: Technologie hochintegrierter Schaltungen [Technology of large-scale integrated circuits], Springer-Verlag, 1988, page 284. Given a customary thickness of the field insulation of about 400 nm, a typical energy range of 250 keV is possible. The typical ion dose of boron atoms is about 10^{13} atoms.

In this exemplary embodiment, the implantations for the NMOS transistor are carried out - for better illustration - in the reverse order to the implantation sequence in a conventional CMOS process, but they can also be carried out in the conventional order.

The first implantation carried out is the NMOS drain implantation of, for example: arsenic, 40 keV, $5.0 \cdot 10^{15}$ atoms. The energy may only be so high that it is masked by the gate electrode in the channel region and the spacer in the LDD region, FIG 3. The spacer is then removed by means of isotropic etching in accordance with Patent Application P 44 15 568.9, and an LDD implantation of, for example: phosphorus, 40 keV, $4 \cdot 10^{13}$ atoms is effected, FIG 4.

Following this, insofar as is necessary and intended, channel implantation of, for example, boron, 60 keV, $4 \cdot 10^{12}$ atoms is carried out, the energy of which is selected such that the range is greater, but not much greater, than the thickness of the gate electrode. Finally, deep implantation, which produces the p-trough, is carried out, FIG 5.

The contacts of the complementary trough are produced at the same time as the implantations for the NMOS transistor. The preferably small, square contact regions 8 in the NMOS mask are exposed for this purpose. As a result of the NMOS drain implantation and the NMOS LDD implantation, a heavily doped region 23 which has the same conduction type as the complementary trough is produced in the region of the surface. The following (in

this exemplary embodiment), deep trough implantation produces, below the contact region 23, a small region in which the complementary trough is redoped. However, said small region prevents the functioning of the substrate contact only to a tenable extent, as long as it does not reach the semiconductor surface. As a result of the preferably small dimensions of the contact regions 8 and the lateral scatter (straggling) of the deep trough implantation, the mean dopant concentration of the trough plug - which is undesired per se - is distinctly less than that of the surrounding (complementary) trough, with the result that they do not reach the semiconductor surface. In the same way that the contact regions for the complementary troughs are opened, by analogy the contact regions of the local trough must remain covered. In a special embodiment, the spacer can be isotropically removed and the LDD implantation can be effected by implantation at an oblique angle of incidence, for example phosphorus, 60 keV, $4 \cdot 10^{13}$ atoms at an inclination of 60° with respect to the semiconductor surface.

Afterwards, the mask 6 is removed and a second mask 30, which defines the PMOS transistors, is produced. The source/drain zones 40 and 41 are produced in a corresponding manner by the implantation of boron ions at typically 10 keV, $5 \cdot 10^{15}$ atoms or BF_2 at 15 keV, $5 \cdot 10^{15}$ atoms. The PMOS transistors are usually designed without any corresponding LDD regions, with the result that they are dispensed with in this exemplary embodiment. Should such implantation be necessary, for example for applications in analog circuits, it is possible to carry out the corresponding process sequence as for an NMOS transistor.

There follows the implantation for the PMOS channel region, for example boron, 60 keV, $3.0 \cdot 10^{12}$ atoms, as well as implantation to improve the transistor punch strength, for example phosphorus, 180 keV, $2.0 \cdot 10^{12}$ atoms.

Finally, the n-type trough is implanted (phosphorus, 500 keV, 10^{13} atoms).

By exposing the complementary contact regions, a contact is analogously produced in the region of the semiconductor surface. The simultaneous trough plug interferes with this function to a tenable extent.

Afterwards, the second transistor mask 30 is removed and the production process is continued in a manner known per se, for example by applying an insulating layer such as BPSG (boron phosphorus silicate glass), which is made to flow in order to level the surface. With the aid of contact holes, the transistor connection zones are made contact with by means of metallization layers to be applied afterwards.

Since, for the production of the NMOS transistor and of the PMOS transistor, the invention requires only one mask in each case, with the aid of which all of the implantations are carried out, the previously customary photographic steps for a self-aligned trough, for the PMOS threshold voltage and for the LDD region of the NMOS transistors can be dispensed with.

Surprisingly, it is shown, in the case of a method according to the invention, that the implantations which are provided with each of the two transistor masks and take place through the polysilicon of the gate 3 and above all through the gate oxide 4 do not significantly impair the quality above all of the gate oxide, with the result that sufficiently reliable transistors can be produced. In tests, it was not possible to ascertain any appreciable deterioration in the intrinsic breakdown strength and any increase in the extrinsic defect density at the typical implantation energies cited.

The problem of the substrate or trough contact is solved in the case of the invention in accordance with FIG 4 in that the trough plugs 11 and 34 formed with the aid of the openings 8 and 32 are situated deep in the substrate, and that above these plugs there are heavily doped zones 23 and 35 which, near to the semiconductor surface between the trough plugs of opposite doping and an associated field insulation region, produce a connection between the trough 33 and the connection 23, on the

one hand, and between the trough 10 and the connection 35, on the other hand. In this case, the trough contact is produced by the different, deep, spatial dopant distribution of the implantations. It is shown that the contact-making of the troughs with the aid of the zones 23 and 25 portrayed is sufficiently good.

From economic aspects, it is shown that the distinctly smaller number of masks in comparison with standard processes as well as the faster physical turnaround times permit a considerable saving in the production of the complementary MOS transistors.

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Patent claims

1. Method for the production of complementary MOS transistors in a substrate, in which each of the complementary transistors is arranged in a corresponding trough and contains a source zone and a drain zone which each adjoin a field insulation zone and define a channel over which a gate oxide and a gate electrode are arranged, characterized by the following steps:

a) the field insulation zones (2), the gate oxide (4) and the gate electrode (3) are produced for each of the complementary transistors,

b) a first mask is used to define a first window (7) for a first transistor of a first conductivity type,

c) the first mask is used to produce a first trough (10) by means of deep implantation of ions of a first conductivity type,

d) the first mask is used to produce heavily doped zones (20, 21, 23) by means of shallow implantation of atoms of a second conductivity type at the substrate surface,

e) the first mask is removed and a second mask (30) is produced which defines a second window (31) for a second transistor of a second conductivity type,

f) the second mask (30) is used to produce a second trough (33, 34) by means of deep implantation of atoms of a second conductivity type,

g) the second mask is used to produce heavily doped zones (40, 41, 35) by means of shallow implantation of atoms of a first conductivity type, and

h) the second mask is removed.

2. Method according to Claim 1, characterized in that the field insulation zones (2) are produced by local oxidation or by structuring an oxide produced with the aid of a CVD process, or by etching shallow trenches in the insulation region and filling them with an oxide.

3. Method according to Claim 1 or 2, characterized in that after the structuring of the gate electrode (3), lateral insulation webs (5) are produced by conformal

deposition and anisotropic etching back of an oxide layer.

4. Method according to Claim 3, characterized in that the insulation webs (5) are in each case isotropically etched after the implantation of the heavily doped zones of the first and second conductivity type (20, 21, 23; 40, 41, 35), and further implantation of atoms of the same conduction type as those of the respective heavily doped zone is carried out with the aid of the respective first and second mask in order to produce lightly doped source/drain zones.

5. Method according to Claim 3, characterized in that the first and the second mask are used to produce in each case lightly doped source/drain zones (24, 25; 42, 43) by means of oblique implantation of atoms of the conduction type of the adjoining heavily doped zones (20, 21, 40, 41).

6. Method according to one of Claims 1 to 5, characterized in that each of the troughs is produced as a retrograde trough.

7. Method according to one of Claims 1 to 6, characterized in that after each trough implantation, shallow implantation of atoms of the same conductivity type as the trough doping is carried out in order to set the transistor threshold voltage.

8. Method according to one of the Claims 1 to 7, characterized in that the first and the second window extends to a point beyond the field insulation regions which are adjacent to the transistor zones.

9. Method according to one of Claims 1 to 8, characterized in that each of the troughs can be made contact with by means of a heavily doped zone, produced at the substrate surface, of the same conductivity type, which zone is produced between two field insulation regions with the aid of an opening (8, 32) provided in the first and second mask, respectively, in the same step as the heavily doped zones (20, 21; 40, 41) of the transistors.