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(57) Abstract

The block diagram illustrates a video signal processing system. It begins with a video disk (10) having a central hole (16) and a track (26). A pickup (28) is positioned to read the track. The signal path includes a PRE AMP (28), a VGA (38), an EQ (40), an A/D (46), and an ADAPTIVE FIR FLTR (48). The output of the filter is connected to a TARGET DET. (81), a TARGET FILTER (50), a WEP DET. (52), a CHUNK SYNC (56), and a BURST DET. (55). A feedback loop is formed by an ERROR (58) block, which receives inputs from the WEP DET. (52) and the CHUNK SYNC (56), and outputs to a TIMING CTL (53) and a GAIN CTL (54). The TIMING CTL (53) also receives input from the A/D (46). The GAIN CTL (54) receives input from the VGA (38). Both the TIMING CTL (53) and the GAIN CTL (54) provide feedback to the A/D (46) and the VGA (38) respectively. A SERVO DRIVER (67) is connected to the pickup (28) and a SERVO CONTROL PROCESS (65). The SERVO CONTROL PROCESS (65) also receives input from the BURST DET. (55) and outputs to the SERVO DRIVER (67) and a SERVO FIELDS DECODER (63). The SERVO FIELDS DECODER (63) also receives input from the BURST DET. (55).