METHOD AND APPARATUS FOR PROCESSING SMALL CORE CELL SIZE SRAM STRUCTURES

FIELD OF THE INVENTION

This disclosure is directed towards a method and apparatus for processing gate and interconnect components, to form small core cell size static random access memory (SRAM) structures.

BACKGROUND OF THE INVENTION

Processes to form ultra large scale integration (ULSI) embedded SRAM products are optimized with respect to several factors including device reliability and yield, device speed, device cell size, process simplicity and cost. The base process to make small SRAM core cells is critical to overall product design. Gate and source/drain interconnect lines play a significant role in controlling both device speed and cell size of SRAM core cells. Two processes commonly used to improve these device properties are the self-aligned silicide (salicide) process and the self-aligned contact (SAC) process.

The salicide process employs metal layer deposition and subsequent annealing (heating) to cause a reaction between the metal and underlying silicon, which forms a low resistivity metal silicide layer at their interface. The salicide process reduces the resistivity of silicon regions, such as polycrystalline silicon (poly-silicon) gates and single crystal silicon source/drain regions, which transport current to other interconnected parts of the device. Reduced resistivity at important gate and source/drain interconnects can improve ULSI logic device speed by reducing the resistance controlled RC time delay. There are drawbacks to integrating a standard salicide process into ULSI logic devices. The salicide process requires isolation spacers between salicide gate and source/drain contacts. Isolation spacers increase the lateral dimension of the core cell according to

standard design rules. Furthermore, the salicide process requires bare silicon surfaces in regions of the device where metal salicidation is desired, and no bare silicon in other regions of the device.

The SAC process combines a dielectric cap layer on top of the poly-silicon gate material and standard dielectric spacers, to completely isolate the gate electrode from subsequent metallization. This eliminates the need to pattern a spacing between the gate electrode and the metallization. Thus, the SAC process reduces SRAM core cell size by forming source/drain contacts that have zero lateral spacing from the gate electrode, without causing a short. However, the dielectric cap on top of the poly-silicon layer renders application of the salicide process difficult. Without a salicide process, the resistivity of some poly-silicon gates is too high for use in a high speed ULSI embedded SRAM device.

Prior embedded SRAM products have typically used a salicide process to form SRAM core cells. These core cells sacrifice some density for higher device speed. A six-transistor complementary metal-oxide-semiconductor (CMOS) SRAM core cell **100**, formed by a salicide process, is illustrated in **Figure 1**. The core cell **100** includes: (1) bit line contacts **106** and **108**; (2) a source/drain contact to V_{dd} **112**; (3) a source/drain contact to ground **118**; (4) source/drain contacts **122**, **124**, **126** and **128**; (5) poly-silicon word line gates **130**; (6) poly-silicon gates **142** and **152**; and (7) horizontal spacings between gate and source/drain contact regions **172**, **174**, **176** and **178**. Bit line source/drain contact **106**, word line gate **130** and source/drain contact **126** comprise a first access transistor. Bit line source/drain contact **108**, word line gate **130**, and source/drain

contact **128** comprise a second access transistor. Source/drain contact **126**, gate **142** and source/drain contact to ground **118** comprise a first driver transistor. Source/drain contact **128**, gate **152** and source/drain contact to ground **118** comprise a second driver transistor. Source/drain contact **122**, gate **142** and source/drain contact to V_{dd} **112** comprise a first load transistor. Source/drain contact **124**, gate **152** and source/drain contact to V_{dd} **112** comprise a second load transistor. Gates **142** of the first load transistor and the first driver transistor are connected; gates **152** of the second load transistor and the second driver transistor are connected; and gates **130** of the first and second access transistors are both connected to a word line.

A six-transistor CMOS structure such as that shown in **Figure 1** can operate as a core cell for an SRAM product. The operation of this type of core cell is well known in the art.

SRAM core cell **100** can be fabricated following standard ULSI device design rules, using a standard poly-silicon gate deposition process such as a salicide process. However, design rules for such a process require that some source/drain contacts (e.g., **122**) be laterally separated from neighboring gates (e.g., **142**), to avoid a short circuit or current leakage between these neighboring transistor components. For 0.25μm technology design rules, a spacing **172** of about 0.2-0.3 μm is required between contact **122** and gate **142**, as shown in **Figure 1**. Similar spacings **174**, **176** and **178** are required between other contacts and gates. The combined extra lateral spacing of about 0.8-1.2 μm corresponds to a significant density loss for a device with a total lateral extent of only 2-3μm.

Thus, there is a need in the art for an improved CMOS process that can reduce the spacings **172, 174, 176** and **178** to zero without causing a short circuit between source/drain contacts **112, 118, 122, 124, 126** and **128**; and gates **142** and **152.** This process should minimize the lateral dimension of an SRAM core cell without sacrificing device speed. This improved process should be compatible with both a standard salicide process and a standard self-aligned contact process. It should minimize changes to either standard process so as to optimize manufacturability and minimize additional cost.

SUMMARY OF THE INVENTION

A method and apparatus to use both an SAC process and a salicide process within a single CMOS process is disclosed. This combined CMOS process minimizes the lateral dimension of an SRAM core cell by using an SAC process to reduce the lateral spacing between most source/drain contacts and gates to zero, without causing a short between them. This combined CMOS process maintains device performance by using a salicide process for source/drain contacts and a few selected gates where low resistivity is most critical to device performance. This combined process minimizes changes to standard salicide and SAC processes, so as to optimize manufacturability and minimize additional cost during fabrication of a wide range of ULSI and embedded SRAM devices.

Embodiments of the combined CMOS process typically begin with series of standard integrated circuit fabrication procedures that include: cleaning and doping the silicon substrate; forming dielectric regions in the silicon substrate that electrically isolate neighboring integrated circuit devices; depositing a gate dielectric material and a polycrystalline silicon gate material onto the silicon substrate; and n-type and p-type doping selected gate regions. These procedures are compatible with standard salicide and SAC processes. A cap layer such as SiO_2 or SiN is then deposited, as for an SAC process. In some embodiments, the cap layer is then selectively etched to define gate regions for salicidation. A subsequent step selectively etches regions of the dielectric cap layer, the poly-silicon gate layer and the gate dielectric layer, as for an SAC process. This process typically continues with source/drain extension, deposition and selective etching of the dielectric spacers, and source/drain doping. The process then proceeds similarly to

a standard salicide process, with metal deposition and annealing. A metal silicide layer is formed by a reaction between the deposited metal and silicon from uncapped gates and source/drain regions. Subsequently, the unreacted metal is stripped. In some embodiments, device processing is the completed by a series of standard integrated circuit fabrication procedures including depositing and selectively etching another dielectric layer, planarizing the device and depositing and selectively etching metallization lines.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features, and advantages of the present invention will be apparent to one skilled in the art, in view of the following detailed description in which:

Figure 1 illustrates a prior art SRAM core cell.

Figure 2 illustrates one embodiment of a high density SRAM core cell.

Figure 3 illustrates a flowchart of one embodiment of a high density SRAM core cell fabrication process.

Figures 4a–4k illustrate the SRAM core cell structure during the fabrication process embodiment described in **Figure 3**.

Figure 5 illustrates features of the SRAM core cell fabrication process embodiment of **Figure 3**.

DETAILED DESCRIPTION OF THE INVENTION

A method and apparatus to process source/drain contacts and gates to form small core cell size SRAM structures is disclosed. In the following description, for purposes of explanation, specific nomenclature is set forth to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention. For example, the embodiments herein are described with reference to a six-transitor CMOS silicon SRAM core cell, but are also applicable to many other device structures.

The disclosed method and apparatus improves performance and increases density of CMOS ULSI devices including embedded SRAM. Some embodiments include a process to form an SRAM core cell including PMOS and NMOS transistors having self-aligned source/drain contacts and self-aligned silicide gates, all in the same device. This disclosed process employs a salicide process without an SAC process in regions of the SRAM core cell where low interconnect resistivity is critical (e.g., word line gates **130** of **Figure 1**). It employs an SAC process without a salicide process in other regions of the core cell where low resistivity is not so critical to device performance (e.g., gate electrodes **142** and **152**, and related source/drain contacts of **Figure 1**). In these regions, spacing loss (**172, 174, 176** and **178** of **Figure 1**) is significantly reduced. The details of this combined process will be described in reference to **Figures 3 and 4**. This combined process requires minimal added process complexity or cost to a standard salicide process, and achieves significant reduction in SRAM core cell size with negligible performance loss.

An embodiment of this combined process may be used to form the high density six-transistor CMOS SRAM core cell **200** illustrated in **Figure 2**. SRAM core cell **200** includes: (1) bit line contacts **206** and **208**; (2) a source/drain contact to V_{dd} **212**; (3) a source/drain contact to ground **218**; (4) source/drain contacts **222**, **224**, **226** and **228**; (5) silicidized poly-silicon word line gates **230**; (6) poly-silicon gates **242** and **252**; and (7) silicidized poly-silicon gate interconnects **245** and **255**. Bit line source/drain contact **206**, a word line gate **230** and source/drain contact **226** comprise a first access transistor. Bit line source/drain contact **208**, a word line gate **230**, and source/drain contact **228** comprise a second access transistor. Source/drain contact **226**, gate **242** and source/drain contact to ground **218** comprise a first driver transistor. Source/drain contact **228**, gate **252** and source/drain contact to ground **218** comprise a second driver transistor. Source/drain contact **222**, gate **242** and source/drain contact to V_{dd} **212** comprise a first load transistor. Source/drain contact **224**, gate **252** and source/drain contact to V_{dd} **212** comprise a second load transistor. Gates **242** of the first load transistor and the first driver transistor are connected through silicidized gate interconnect **245**. Gates **252** of the second load transistor and the second driver transistor are connected through silicidized gate interconnect **255**. Silicidized gates **230** of the first and second access transistors are both connected to a word line.

The operation of high-density core cell **200** is identical to that of core cell **100**, and is well known in the art. However, high-density core cell **200** is different, in that some source/drain contacts and gates (e.g., source/drain contact **226** and gate **242**) appear to be in contact. Nevertheless, they remain electrically isolated owing to vertical

displacement, as will be described in reference to **Figure 5**. This structural change eliminates spacings **172, 174, 176, and 178** of **Figure 1**, which results in a core cell size reduction and corresponding device density increase of about 30%. The trade-off for this improvement is that regions **242** and **252** comprise higher resistivity unsilicidized poly-silicon, in contrast to regions **142** and **152** of **Figure 1**. Fortunately, regions **242** and **252** do not participate in long distance current flow, so only a slight performance degradation results. Low resistivity is critical to device performance in regions **230, 245** and **255**. Fortunately, these regions are separated from source/drain contacts **112, 118, 122, 124, 126,** and **128**, and so can undergo salicidation without increasing spacings **172, 174, 176,** and **178**.

Figure 3 illustrates a flowchart of a process **300** used by some embodiments of the invention. This process **300** can form the silicidized and unsilicidized poly-silicon gates of SRAM core cell **200**. As shown in **Figure 3**, process **300** proceeds as follows: (**310**) Carry out standard CMOS process steps including substrate doping and a transistor isolation process; (**320**) deposit gate dielectric and poly-silicon gate materials; (**330**) N+ pre-dope selected poly-silicon gate regions; (**340**) P+ pre-dope selected poly-silicon gate regions; (**350**) deposit cap layer; (**360**) selectively etch selected cap layer regions; (**370**) selectively etch selected regions of the gate dielectric, poly-silicon gate and dielectric cap material layers; (**380**) deposit and selectively etch dielectric spacers; (**390**) deposit metal, anneal to form silicide layer, and remove unreacted metal; and (**395**) deposit dielectric, planarize, and complete standard CMOS processing steps.

Each of the operations of process **300** will now be further described by reference to **Figures 4a-4k**. **Figures 4a-4k** illustrate device structures **400** after each step of process **300**.

Figure 4a illustrates the device structure **410** after step **310** of process **300**. Structure **410** includes: (1) a silicon substrate **412**; and (2) a substrate dielectric material **414**. Silicon substrate **412** is prepared, prior to step **310**, by standard CMOS procedures compatible with SAC and salicide processes. These procedures typically include cleaning and doping. Substrate dielectric material **414** is formed in silicon wafer **412** by an isolation process **310** such as shallow trench isolation, LOCOS isolation or PBLOCOS isolation. Substrate dielectric material **414** electrically isolates device components within the silicon wafer, such as a source and a drain of neighboring transistors.

Figure 4b illustrates the device structure **420** after step **320** of process **300**. Structure **420** includes: (1) silicon substrate **412**; (2) substrate dielectric material **414**; (3) a gate dielectric material **422**; and (4) a poly-silicon gate material **424**. Gate dielectric material **422** is formed first, and a poly-silicon gate material layer **424** is deposited on top of gate dielectric material **422**. The gate dielectric material **422** electrically isolates the poly-silicon gate material **424** from device components in the silicon substrate **412**.

Figure 4c illustrates the device structure **430** after step **330** of process **300**. Structure **430** includes: (1) silicon substrate **412**; (2) substrate dielectric material **414**; (3) gate dielectric material **422**; (4) poly-silicon gate material **424**; and (5) a selectively etched photoresist region **432**. Photoresist region **432** protects the underlying region of

poly-silicon gate material **424** from subsequent doping. Photoresist region **432** defines an N+ pre-doped region of poly-silicon gate material **424**, at step **330**, by a masking process. The masking process includes blanket deposition of photoresist and exposure of a portion of the photoresist to allow selective removal of a portion of the photoresist. In this manner, a region of the poly-silicon gate material layer is selected for subsequent n+ type doping as shown. Doping typically comprises a dose of between $1*10^{14}$ ions/cm^2 and $5*10^{15}$ ions/cm^2 of phosphorous or arsenic. After doping, the remaining photoresist **432** is removed.

Figure 4d illustrates the device structure **440** after step **340** of process **300**. Structure **440** includes: (1) silicon substrate **412**; (2) substrate dielectric material **414**; (3) gate dielectric material **422**; (4) poly-silicon gate material **424**; and (5) a selectively etched photoresist region **442**. At step **340**, photoresist region **442** enables P+ pre-doping of selected regions of poly-silicon gate material **424**, by a masking process similar to that of step **330**. Doping typically comprises a dose of between $1*10^{14}$ ions/cm^2 and $5*10^{15}$ ions/cm^2 of boron, BF_2 or Indium.

Figure 4e illustrates the device structure **450** after step **350** of process **300**. Structure **450** includes: (1) silicon substrate **412**; (2) substrate dielectric material **414**; (3) gate dielectric material **422**; (4) poly-silicon gate material **424**; and (5) a dielectric cap layer **452**. A 500-5000Å dielectric cap layer **452**, such as SiO_2, SiN, or a combination thereof, is deposited (at step **350**) on top of the poly-silicon gate layer **424**.

Figure 4f illustrates the device structure **460** after step **360** of process **300**. Structure **460** includes: (1) silicon substrate **412**; (2) substrate dielectric material **414**; (3) gate dielectric material **422**; (4) poly-silicon gate material **424**; (5) regions of the dielectric cap layer **452** and; (6) selectively etched regions of a photoresist material **464**. Photoresist material **464** protects regions of dielectric cap layer **452** from subsequent etching. Regions of dielectric cap layer **452** are removed, at step **360**, by a selective etching process. This etching process forms regions of bare poly-silicon gate material **424** and regions of poly-silicon gate material **424** capped by dielectric cap material **452**. Regions of the structure **460** with the dielectric cap **452** will undergo SAC processing. Regions of the structure **460** with bare poly-silicon gate material **424** will undergo salicide processing.

Figure 4g illustrates the device structure **470** during step **370** of process **300**. Structure **470** includes: (1) silicon substrate **412**; (2) substrate dielectric material **414**; (3) gate dielectric material **422**; (4) poly-silicon gate material **424**; (5) regions of the dielectric cap layer **452** and; (6) selectively etched regions of a photoresist material **472**. Photoresist material **472** protects regions of dielectric cap layer **452**, poly-silicon gate material **424**, and gate dielectric material **422** from subsequent etching.

Figure 4h illustrates the device structure **475** after step **370** of process **300**. Structure **475** includes: (1) silicon substrate **412**; (2) substrate dielectric material **414**; (3) regions of gate dielectric material **476**; (4) regions of poly-silicon gate material **477**; and (5) regions of dielectric cap layer **478**. The dielectric cap layer **452**, the poly-silicon gate

layer **424** and the gate dielectric layer **422** are removed (at step **370**) from regions not covered by photoresist **472**. The resulting structure **475** includes regions of bare silicon substrate **412**; regions of silicon substrate **412** covered by gate dielectric material **476** and poly-silicon gate material **477**; and regions of silicon substrate **412** covered by gate dielectric material **476**, poly-silicon gate material **477**, and dielectric cap material **478**. Important standard process steps for source/drain extension and pocket implantation (not shown) are also performed during step **370**, after structure **475** is defined.

Figure 4i illustrates the device structure **480** after step **380** of process **300**. Structure **480** includes: (1) silicon substrate **412**; (2) substrate dielectric material **414**; (3) regions of gate dielectric material **476**; (4) regions of poly-silicon gate material **477**; (5) regions of dielectric cap layer **478**; and (6) dielectric spacers **482**. Dielectric spacers **482** are formed, at step **480**, by deposition of a dielectric material and a selective etching process. The combination of dielectric cap layer **478** and dielectric spacers **482** isolates selected regions of poly-silicon gate material **477** from subsequent processing and metallization. Important standard process steps for source and drain formation (not shown) are also performed during step **380**, after structure **480** is defined.

Figure 4j illustrates the device structure **490** after step **390** of process **300**. Structure **490** includes: (1) silicon substrate **412**; (2) substrate dielectric material **414**; (3) regions of gate dielectric material **476**; (4) regions of poly-silicon gate material **477**; (5) regions of dielectric cap layer **478**; (6) dielectric spacers **482**; and (7) metal silicide regions **492**. Metal silicide regions **492** are formed, at step **390**, by a salicide process.

During the salicide process, a low resistivity silicide forming material, such as titanium, cobalt or nickel is deposited (e.g., sputter deposition of between 100 Å and 500Å of titanium), and the silicon substrate is annealed (e.g., by rapid thermal processing for between1 and 30 seconds at between 500°C and 1000°C. The metal in direct contact with silicon reacts to form metal silicide regions **492**. Metal in direct contact with dielectric materials (**478** and **482**) does not react, and is subsequently etched away.

Figure 4k illustrates the device structure **495** after step **395** of process **300**. Structure **495** includes: (1) silicon substrate **412**; (2) substrate dielectric material **414**; (3) regions of gate dielectric material **476**; (4) regions of poly-silicon gate material **477**; (5) regions of dielectric cap layer **478**; (6) dielectric spacers **482**; (7) metal silicide regions **492**; and (8) a dielectric material **496**. At step **395**, a dielectric material such as BPSG **496** is deposited, planarized, and selectively etched, to form structure **495**. When cap layer **478** is SiO_2, a liner layer such as SiN may be deposited prior to BPSG **496** deposition.

Figure 5 illustrates features of an embodiment of device structure **500** formed by process **300**. Device structure **500** includes (1) silicon substrate **505**, (2) substrate dielectric isolation **510**, (3) dielectric gate isolation **515**, (4) metal silicide layer **520**, (5) poly-silicon gate electrodes **525**, (6) dielectric spacers **530**, (7) cap layer **535**, (8) BPSG isolation layer **540**, and (9) contact metallization **545**.

Device structure **500** minimizes CMOS SRAM core cell size by a self-aligned contact (SAC) process that reduces the horizontal spacing between selected transistor gate

electrodes and their source/drain metal contacts to zero. In this SAC process, gate electrodes **525** are isolated from source/drain contact metallization **545** by dielectric spacers **530** and dielectric cap layer **535**. The horizontal spacing between these gate electrodes **525** and the metal contacts **545** is zero, at boundaries **550** marked by thick vertical lines in **Figure 5**. Zero spacing for these SAC gate structures (such as gate structures **570**, **575** and **580**) is less than the spacing needed for a gate structure formed by a salicide process, such as gate structure **585**. The space saving SAC structure is desirable for the access and driver transistors of **Figure 2**. SAC processing in these regions (**242** and **252** of **Figure 2**) eliminates the need for spacings **172**, **174**, **176**, and **178** of **Figure 1**.

Device structure **500** maintains high SRAM processing speed by using a low resistivity salicide process gate structure, such as gate structure **585**, where necessary to match a low resistivity peripheral circuit. Salicide processing in these regions (**230**, **245**, and **255** of **Figure 2**) maintains overall device performance at near that of a lower density device using a standard salicide process for all gates.

Low resistivity metal silicide **520**, formed by a salicide process, is also used at source/drain contacts between the silicon substrate **505** and the metallization **540**, at interfaces **560** marked by heavy dashed lines. Performance of source/drain contacts, thus, also matches devices made by a standard salicide process.

This method and apparatus for processing source/drain, gate and interconnect components, to form small core cell size SRAM structures, has several advantages over the prior art. It enables compatible use of both self-aligned contact and salicide processes

within a single CMOS process. It minimizes the lateral dimension of an SRAM core cell by using a self-aligned contact process that reduces the lateral spacing between the source/drain contacts and the gates to zero, without causing a short between them. It maintains high conductivity metal silicide, by a salicide process, where necessary to match the high conductivity of peripheral circuits. This CMOS process also minimizes changes to standard salicide and self-aligned contact processes, so as to optimize manufacturability and minimize additional cost.

The foregoing has described new methods and apparatus for processing poly-silicon gate and interconnect components, to form small core cell size SRAM structures. Although the invention is described with respect to a preferred embodiment, modifications thereto will be apparent to those skilled in the art. It is contemplated that changes and modifications may be made to the materials and arrangements of elements of the present invention without departing from the scope of the invention. Therefore, the scope of the invention is to be determined by reference to the claims that follow.



CLAIMS

We claim

1. A method of fabricating an integrated circuit device, said method comprising:

a) depositing a gate dielectric material and a gate material on a silicon substrate;

b) depositing a dielectric cap material, and selectively etching regions of said dielectric cap material;

c) selectively etching regions of said gate dielectric material, said gate material and said dielectric cap material to form gate electrodes;

d) depositing a spacer dielectric material, and selectively etching regions of said spacer dielectric material;

e) depositing a metal layer material and annealing to form a metal silicide layer at regions of contact between said metal layer material and at least one of said gate material and said silicon substrate; and

f) removing unreacted metal layer material.

2. The method as claimed in claim 1, further comprising:

forming device isolation areas on said silicon substrate prior to step a);

n-type and p-type doping selected regions of at least one of said silicon substrate and said gate material prior to step b);

performing processing steps prior to step e), including source/drain extension, pocket implantation and source/drain doping; and

depositing a dielectric material, planarizing, and completing standard CMOS processing steps after step f).

3. The method as claimed in claim 1, wherein:

gate electrodes located in regions etched during step b) include metal silicide; and

gate electrodes located in regions not etched during step b) include polycrystalline silicon.

4. The method as claimed in claim 3, wherein said regions etched during step b) undergo a self-aligned silicide process and said regions not etched during step b) undergo a self-aligned contact process.

5. The method as claimed in claim 1, wherein said dielectric cap material and said spacer dielectric material comprise a high resistance boundary between a source/drain contact and a gate electrode.

6. The method as claimed in claim 5, wherein said source/drain contact and said gate electrode are separated in a vertical direction that is defined by the plane normal of said silicon substrate, and have one of zero horizontal separation and horizontal separation less than that permitted by standard integrated circuit fabrication design rules.

7. The method as claimed in claim 5, wherein said source/drain contact undergoes a self-aligned silicide process to form a metal silicide.

8. The method as claimed in claim 2, wherein said doping selected regions comprises N+ doping with a dose between $1*10^{14}$ ions/cm^2 and $5*10^{15}$ ions/cm^2 of one of phosphorous and arsenic and P+ doping with a dose between $1*10^{14}$ ions/cm^2 and $5*10^{15}$ ions/cm^2 of one of boron, BF_2 and Indium.

9. The method as claimed in claim 3, wherein said metal layer material comprises one of titanium, cobalt and nickel and said metal silicide comprises one of titanium di-silicide, cobalt di-silicide and nickel mono-silicide.

10. The method as claimed in claim 3, wherein said depositing a metal layer material and annealing to form a metal silicide layer comprises depositing between 100Å and 500Å of titanium and rapid thermal processing for between 1 and 30 seconds at between 500°C and 1000°C, to form titanium di-silicide.

11. A method for fabricating an integrated circuit device comprising:

a self-aligned contact process including:

depositing a gate dielectric material, a gate material, and a dielectric cap material on a silicon substrate;

selectively etching regions of said gate dielectric material, said gate material and said dielectric cap material; and

depositing a spacer dielectric material, and selectively etching regions of said spacer dielectric material;

a process of selectively etching regions of said dielectric cap material; and

a self-aligned silicide process including:

depositing said gate dielectric material and said gate material on said silicon substrate;

depositing said spacer dielectric material, and selectively etching regions of said spacer dielectric material;

depositing a metal layer material and annealing to form a metal silicide layer at regions of contact between said metal layer material and at least one of said gate material and said silicon substrate; and

removing unreacted metal.

12. The method as claimed in claim 11, wherein:

said selectively etching regions of said dielectric cap material is performed during said self-aligned contact process prior to said selectively etching regions of said gate dielectric material, said gate material and said dielectric cap material; and

said self-aligned silicide process is performed in regions of said device wherein said etching regions of said dielectric cap material is performed.

13. The method as claimed in claim 11, wherein said self-aligned contact process forms a polycrystalline silicon gate electrode and a self-aligned source/drain contact.

14. The method as claimed in claim 13, wherein said polycrystalline silicon gate electrode has zero horizontal spacing from said self-aligned source-drain contact.

15. The method as claimed in claim 13, wherein said self-aligned silicide process forms a gate electrode including a metal silicide.

16. An integrated circuit device comprising:

a self-aligned source/drain contact;

a first gate including a metal silicide region; and

a second gate having zero horizontal spacing from said self-aligned source/drain contact.

17. The apparatus as claimed in claim 16, wherein said first gate including a metal silicide region comprises one of a metal silicide formed by a self-aligned silicide process and polycrystalline silicon in contact with a metal silicide formed by a self-aligned silicide process.

18. The apparatus as claimed in claim 16, wherein said second gate and said self-aligned source-drain contact are formed by a self-aligned contact process.

19. The apparatus as claimed in claim 16, wherein a word line gate comprises a first gate and at least one of an access transistor gate and a driver transistor gate comprises a second gate.