# PATENT SPECIFICATION (11) 1 574 511

1 574 511

(21) Application No. 3024/77 (22) Filed 25 Jan. 1977
(31) Convention Application No. 51/146 512
(32) Filed 8 Dec. 1976 in
(33) Japan (JP)
(44) Complete Specification published 10 Sept. 1980
(51) INT CL³ G01N 21/88
(52) Index at acceptance
G1A A9 AJ C10 C1 C4 C8 D10 D1 D4 G12 G17 G1 G2 G6 MB P14 P16 P17 R7 S3 T15 T25 T3 T4 T8 T9
H1K MA


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## (54) METHOD AND APPARATUS FOR AUTOMATICALLY INSPECTING AND CORRECTING MASKS


(71) We, HITACHI, LTD., of 5—1, 1-chome, Marunouchi, Chiyoda-ku-Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—


This invention relates to method and apparatus for automatically inspecting and correcting photomasks used in the semiconductor industries.

In the manufacture of semiconductor devices and integrated circuit (IC) devices, there exist steps of forming an oxide film pattern of desired shape on a thin semiconductor wafer and diffusing impurity atoms into the regions not covered with the oxide pattern or of forming a desired wiring pattern of aluminium, etc. Such an oxide or aluminium pattern is formed in the following way. First, an oxide or aluminium film is deposited on the whole surface of a semiconductor wafer and then a photoresist film is coated thereon. A photomask is disposed on the semiconductor wafer in close contact thereto or with a predetermined gap therefrom. Ultraviolet light is irradiated on the photoresist film through the photomask to sensitize the photoresist film. The sensitized or non-sensitized regions of the photoresist film are removed by etching to leave a photoresist pattern. The oxide or aluminium film on the water surface is subjected to an etching treatment using the remaining photoresist pattern as a mask, thereby forming an oxide or aluminium pattern.

The quality of such oxide pattern or aluminium wiring pattern dominates the yield and the reliability of the semiconductor devices. Therefore, such patterns should be formed with high accuracy.

The quality of the oxide or aluminium pattern is largely dominated by the quality of the photomask. Therefore, the pattern in the photomask is desired to be formed very precisely prior to the manufacture of the semiconductor device. There arises a need for inspecting the pattern of the manufactured mask and correcting defective portions if any.

Conventionally, chromium patterns deposited on glass plates have been used as correctable masks. Defective portions in the chromium mask are generally inspected by the following methods:

(1) Eye-measurement method or visual inspection of inspecting defective portions in a mask by eye measurement using a mask analyzer;

(2) Method of comparing two chip patterns in a mask through photoelectrically converted signal and discriminating defective portions by the difference in the photoelectrically converted signals (see the article by Bruning, Sitting: entitled "An Automated Mask Inspection System"; IEE Vol. ED22, No. 7, p.p. 847 to 495, July 1975)

(3) Method of Fourier-transforming the mask pattern and subtracting irregular defective portions by filtering (see the article by L. S. Watkins: entitled "Application of Spatial Filtering Subtraction to Thin Film and IC Mask Inspection"; Appl. Opt. Vol. 12, p. 1880, 1973).

These methods are accompanied with respective drawbacks; method (1) has drawbacks that some defective portions may be over-looked and that the time required for inspection is long, method (2) has drawbacks that minute defectives smaller than 2 $\mu$m cannot be detected and there is some danger of mis-discriminating normal portions as defective portions, and method (3) has a drawback that there is no direct correspondence between the defect detection and the positional identification. More particularly, according to method (2) the video signals for the two chip patterns cannot be perfectly synchronized but there exists some time lag due to the positional displacement of the two normal chip

25 OCT 1982

patterns within the tolerance which may differ one from another. Thus, defective portions smaller than the maximum tolerance cannot be detected. If the detection threshold is lowered to raise the detection accuracy, some normal portions may be discriminated as defective ones. On the other hand according to method (3) the information of the normal pattern is erased in the filtering process. Therefore, there remains no correspondence between the mask pattern and the detected defective portions. Only the existence of some defective portions in a mask pattern can be detected and there is a gap for correcting the detected defective portions in the mask pattern. Thus, the total operation efficiency is very low.

According to one aspect of the present invention there is provided a method of inspecting masks used in forming a desired oxide pattern or a desired wiring pattern on a semiconductor wafer and wherein each mask is formed from a layer of an opaque material deposited in a predetermined pattern on a surface of a transparent substrate, a portion of the layer of the opaque material being designed to have a predetermined minimum pattern width; the method comprising the steps of;

mounting a pair of similar masks on a mounting stage;

converting images of the patterns of the masks into electrical video signals respectively;

converting said electrical video signals into binary signals on the basis of at least one reference threshold value;

storing a plurality of bits of said binary signals corresponding to said minimum pattern width;

comparting the central bit of stored binary signals with the each end bit of the stored binary signals so as to detect a minute portion (as hereinbefore defined); and

detecting defects in at least one of the masks by comparing the results of detecting minute portions in said two patterns so as to cancel signals representing the common minute portions and leave a signal representing minute portions existing in one only of the two patterns.

According to a second aspect of the present invention there is provided an apparatus for inspecting the pattern of a mask of the type used in forming a desired oxide pattern or a desired wiring pattern on a semiconductor wafer and of the type formed from a layer of opaque material deposited in a predetermined pattern on a surface of a transparent substrate a portion of the layer of opaque material being designed to have a predetermined minimum pattern width in order to detect a defective portion therein including;

means for mounting a pair of masks in a predetermined positional relation to each other and for shifting said pair of masks in a plane by the same amount;

a pair of opto-electrical converter means located in a predetermined positional relation with said mask mounting means for converting received images of the mask patterns into electrical video signals;

optical means for directing light on to said pair of masks and for focusing the images of said pair of patterns on said pair of opto-electrical converter means;

a pair of binary-coding means for transforming the electrical video signals from said converter means into respective binary signals;

a pair of memory circuits for storing a respective plurality of bits of the binary signals corresponding to the minimum pattern width and

a detecting circuit which compares the central bit with each end bit in each plurality of stored binary signals so as to detect a minute portion (as hereinbefore defined), and which compares the results of detection of the minute portions in the two patterns so as to cancel signals representing the common minute portions and leave minute portions existing in one only of the two patterns.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:—

Figure 1 is a flow chart illustrating the outline of the automatic mask inspection and correcting according to this invention.

Fig. 2 is a perspective view showing a group of units to be used in the automatic mask inspection and correction according to an embodiment of this invention.

Figs. 3a and 3b are illustrative views for expanding the inspection of a pair of masks in which; Fig. 3a is a top view of a pair of masks with illustration of scanning traces and Fig. 3b is a partial perspective view of an area control means for defining the scanning area.

Fig. 4 is an illustrative drawing showing how the patterns of a pair of masks are converted into electrical signals and electrically processed to inspect any defective portions.

Fig. 5a is a block diagram showing an example of binary-coding a video signal utilizing three theshold values; Fig. 5b is a circuit diagram showing the details of Fig. 5a; and Fig. 5c is a flow chart of the logic circuit in Fig. 5a.

Fig. 6 is a schematic diagram showing the relation of a photodiode array and a pattern under reading.

Figs. 7a to 7c are schematic diagrams showing bit structures used for detecting minute portions.

Fig. 8a and 8b are schematic diagrams showing critical cases of coding a pattern into binary signals, and Figs. 8c to 8e are schematic diagrams of bit structures used for parallel-out memories.

Figs. 9a, 9b, 10a and 10b are schematic diagrams of bit structures used for the parallel-out memories.

Fig. 11 is a block diagram of a defect discriminating circuit to be used in the system of Fig. 4.

Fig. 12 is an illustrative diagrams for explaining the minute pattern comparison method and the boundary comparison method.

Fig. 13 is a schematic diagram showing the memory content in a magnetic tape.

Fig. 14 is a schematic side view of a pattern correcting device using a laser beam.

Figs. 15a to 15c, and 16a to 16c are schematic diagrams of bit structures for detecting boundaries.

Fig. 1 is a flow chart of the method of automatically inspecting and correcting masks according to this invention. As shown in the figure, a pair of manufactured masks are subjected to pattern inspection to detect defective portions. The detected defective portions are recorded in a recording medium such as a magnetic cassette tape using a recording device. Then, the data of the defective portions recorded in the cassette tape are read out and used for identifying the defective portions in a pattern correcting device.

Fig. 2 shows a group of processing devices, in which are shown from the left-hand side of the righthand side of a control unit 1 including a memory device, a mask inspection unit 2, a light exposure device 3 which forms part of the pattern correcting unit, a read-out control device 4 for reading out the information of a defective portion and an etching device 5 which constitute part of the pattern correcting unit. The control unit 1 contains from the upper side to the lower side a synchroscope 6 for monitoring the video signal of the mask pattern, a mount 7 for loading a cassette tape, a detection circuit 8 for electrically detecting the patterns of a pair of masks and discriminating the existence of a defective portion, an automatic focusing circuit 9 for driving a mask and focusing the objective lens on the mask and a power source circuit 10. The mask inspection unit 2 includes a support carrier 11, an xy scanning stage 14 mounted on the carrier 11 and mounting a pair of masks 13 in juxtaposition to each other on mask holders 12, a column 15 extending upwardly from one side portion of the carrier 11 and a support box 16 fixed on the column 15, and an optical system comprising a pair of objective lens systems 17 and a pair of eye lens systems 18. The xy-scanning stage 14 is movable in the longitudinal and the transverse directions on a horizontal plane, i.e. x- and y-directions, and also in the vertical direction, i.e. z-direction. The stage 14 is translated by a scanning motor 19. The movement of the xy-scanning stage 14 is controlled by an inspection area control means 20. A linear encoder 21 and an automatic focusing motor 22 are also provided on the xy-scanning stage 14. An image pick-up means including a pair of arrays 23 of photodiodes is disposed in the support box 16.

Processes or procedures for inspecting the patterns of a pair of masks will be described next. First, a pair of masks 13 to be inspected are prepared and set on the xy-scanning stage 14. Then, the automatic focusing motor 22 is controlled to bring the distance from the mask to the objective lens at a predetermined value to achieve focusing. This process is for the purpose of projecting the image of the mask pattern on the photodiode array in the correctly focused state. Then, as shown in Fig. 3a, the xy-scanning stage 14 is moved in zig-zag form as shown by arrows for picking up the total images of the respective mask patterns by the photodiode arrays 23. Here, since the semiconductor wafers are usually in circular shapes, the utilization area in the mask pattern formed on the mask 13 is usually circular as shown by the dotted broken line in Fig. 3a corresponding to the wafer shape. Therefore, for reducing the inspection period, the image pick-up process by the photodiode array may be achieved only on the utilization area of the mask pattern 13, i.e. in the circular area. To facilitate such function, the inspection area control means 20 is provided on the xy-scanning stage 14. Fig. 3b shows the outline of the manner of controlling the scanning of the xy-scanning stage utilizing the scanning area control means 20. This scanning area control means 20 comprises a templet 26 formed by depositing a chromium layer 25 on the lower surface of a transparent glass plate 24 except a circular region, a light source 27 for projecting light on the surface of the templet deposited with the chromium layer 25 and a light detector 28 provided with a slit 29 for receiving the lights emitted from the light source 27 and reflected by the chromium layer 25. The templet 26 is attached on the xy-scanning stage 14 in such a manner that the position on the templet 26 irradiated by the light source 27 and reflecting light to the detector 28 corresponds to the position in the mask 13 the image of which is picked up by the photodiode array. The light source 27 and the light detector 28 are fixedly mounted on the carrier 11 with a predetermined distance

separated from each other to be disposed beneath the templet 26. The slit 29 is so adjusted that the detector 28 receives only lights emitted from the light source 27 and reflected by the templet 26 with sufficient accuracy. When, the x-scanning stage is translated in the direction indicated by arrow A shown in Fig. 3b, light is emitted from the source 27 onto the templet. Neglecting the reflectance of glass in comparison with that of chromium, the light detector 28 receives no light and the scanning of the x-stage proceeds while the circular portion of the templet 26 is scanned. Along with the scanning, the light reflected by the chromium layer 25 starts to enter the slit 29. Then, the detector 28 generates a detection signal and the scanning is stopped. Then the y-stage is translated or moved by one field of view of the photodiode array. Then, the x-stage is translated in the opposite direction to the previous one, i.e. in the direction indicated by arrow B shown in Fig. 3b. Similar steps are repeated to scan the whole area in the circle. Thus, defective portions in the circular areas of the photomasks are inspected by moving the xy-scanning stage and picking up the images of patterns of the photomasks in the circular area by the photodiode arrays.

Next the conversion of the mask pattern into an electrical signal and detection or defective portions from the electrical signal will be described.

Fig. 4 shows how the defective portions are inspected. In the figure, a light source 30 of high brightness or liminance may be a 250 W mercury lamp. The light from the light source 30 is reflected by mirrors 31 and 32, condensed by condenser lenses 33 and 34 and projected on the masks 13A and 13B. The light transmitted through the masks 13A and 13B and carrying the pattern information is directed on the photodiode arrays 23A and 23B through the objective lenses 17A and 17B. Each of the photodiode arrays 23A and 23B is formed of a linear alignment of 256 photodiodes each having a dimension of 25.4 $\mu$m square. Here, for obtaining a resolution of 1 $\mu$m square, an expanded image, 25 times as large as the mask pattern, is focused on the photodiode array. Photodiodes of the arrays 23A and 23B are aligned in y-direction of the xy-scanning stage. The xy-stage carrying the photomasks is driven in x-direction in the zig-zag manner as described above to provide the information of two-dimensional pattern. Light arriving at the photodiode array is converted into video signals, each having a voltage corresponding to the intensity of the light transmitted through the mask pattern in the unit area of 1 $\mu$m square. The photodiode arrays are activated by clock (timing) pulses. Each video signal corresponds to the area of 1 $\mu$m square in the mask pattern. The video signals are amplified by amplifiers 54A and 54B and the amplified signals are supplied to comparators 55A and 55B. The comparators compare the input signals with a group of constant threshold values and quantize the input signals into binary signals, for example one having the levels of 5 V and 0 V corresponding respectively to the white and black of the pattern i.e. absence and existence of the chromium mask in the detected area. Voltage sources 56A and 56B supply the threshold voltages to the comparators for binarycoding 55A and 55B. As the pattern becomes finer, namely, as minute portions such as excess chromium portions and pinholes in the chromium layer of the mask pattern are photoelectrically detected, a definite video signal becomes unintelligible and the binary coding of the pattern on the basis of one threshold value becomes difficult. Therefore, three threshold values, namely, high, middle and low threshold voltages of 1.7 V, 1.4 V and 1.1 V respectively are provided in this embodiment and the video outputs using these three threshold values are logically processed to select a gate for generating the binary signal, in the manner as shown in Figs. 5a to 5c. The selection of the gate, i.e., a binary coded signal is determined from the history of succeeding five bits including preceding two bits, the bit under inspection and the following two bits on a time base.

In Fig. 5a, each of the above-mentioned comparators for binary-coding 55A and 55B comprises a threshold generator VG, as simply indicated by 56A or 56B, for providing three constant potentials of 1.1 V, 1.4 V and 1.7 V, which provide thresholds of a dark level, a normal level and a bright level for the detected video signal respectively. The binary coding device comprises threshold comparators $C_1$, $C_2$ and $C_3$ connected in each input to the different outputs of the threshold generator VG, respectively. The threshold comparators are formed of usual operation amplifiers, which may be of the type LM306 manufactured by National Semiconductor Corp. As the other comparison input, a video signal is applied to each threshold comparator through video amplifier 54A and 54B from the photodiode array 23A or 23B. From theshold comparators $C_1$, $C_2$ and $C_3$ threshold-dependent bit signals "1" and "0" are developed for the high "H", middle "M", and low "L" thresholds and supplied to five-bit shift registers $SR_1$, $SR_2$ and $SR_3$, respectively. The five-bit shift register may be of the type HD2546, manufactured by Hitachi Limited. A gate selector S includes

a logic circuit which comprises NAND gates of the types HD7430, HD7440 and inverters of the type HD7404 which are IC function units manufactured by Hitachi, Ltd. The logic circuits of the gate selector are connected to receive parallel-out bit signals from the shift registers $SR_1$, $SR_2$ and $SR_3$ and performs a predetermined logic operation to determine the selection of a gate to be operated with respect to the threshold-dependent bit signals at the third bit positions, i.e., the central digit position of the shift registers $SR_1$, $SR_2$ and $SR_3$. The logic circuit of the gate selector S is constructed to operate in the manner shown by the flow chart in Fig. 5c. In the flow chart, the symbols "M", "H" and "L" respectively denote middle, high and low threshold-dependent bit signals which are suppled from the corresponding shift registers in Five-bit parallel-out form. AND gates $G_1$, $G_2$ and $G_3$ are provided to be actuated by a selection signal from the gate selector S which is provided as a result of the logic operations as described in the flow chart. The AND gates $G_1$, $G_2$ and $G_3$ are applied with outputs at the third bit positions of the shift registers $SR_1$, $SR_2$ and $SR_3$, either one of which is selected by the gate selection signal to pass a corresponding one of the "M", "H" and "L" threshold-dependent bit signals through an OR gate as a binary coded signal at an output terminal of the binary coding circuit 55A (or 55B). Then the binary coded signal thus converted from the input video signal is applied to the serial memory 57A (or 57B).

The details of the binary coding circuit of Fig. 5a are shown in Fig. 5b by way of example, in which the threshold voltage ($V_{th}$) generator comprises potentiometers $VR_1$, $VR_2$ and $VR_3$ for "H", "M" and "L" thresholds. The gate selector S indicated in the block achieves a logic shown in the flow chart of Fig. 5c. Parallel bit outputs of the shift register $SR_1$ respectively connected through respective inverters $A_4$ to NAND $B_5$, the output of which is supplied to a first NAND $E_6$ and a first NAND $G_6$, and to two NANDs $C_6$ and a second NAND $E_6$ through a first inverter $G_5$. Parallel five-bit outputs of shift registers $SR_2$ are applied to NAND gate $F_5$ and through inverters $D_5$ to NAND gate $E_5$. The outputs of NAND gates $F_5$ and $E_5$ are applied to NAND $D_5$, the output of which is applied to first NAND $E_6$ and through a second inverter $G_5$ to second NAND $E_6$ of the gate 2. Parallel five-bit outputs of the shift register $SR_3$ are applied to NAND $H_5$, the output of which is supplied to one NAND $G_6$ of gate $G_3$ and one NAND $C_6$ of gate $G_1$ through a third inverter $G_5$ and directly to the other NAND $G_6$ and the other NAND $C_6$ of gate $G_1$. The third bit signal $AH_3$ of $SR_1$ is supplied to the first NAND $G_6$ and the first NAND $E_6$, the third bit signal $AM_3$ or $SR_2$ to the second NAND $G_6$, and the third bit signal $AL_3$ of $SR_3$ to the second NAND $C_6$ and the second NAND $E_6$. In the gates $G_1$, $G_2$ and $G_3$, outputs of pairs of NANDs $C_6$, $E_6$ and $G_6$ respectively are applied to corresponding NANDs $M_6$ as OR gate of Fig. 5a, the output of which develops a binary coded signal to be supplied to the memory 57A (or 57B).

The binary coded signals are then recorded in serial memories 57A and 57B, each consisting of shift registers of 256 × 15 bits and then in parallel-out memories 58A and 58B, each consisting of shift registers of 15 × 15 bits.

The algorithm of determining a defective portion will now be described briefly, with reference to Fig. 12. A minute portion is herein defined as a pattern smaller that the minimum pattern width in the mask pattern.

One method of determining a defective portion is to use the minute comparison method. With this method, patterns are divided into small segments, each having a width smaller than the minimum pattern width of a designed pattern and a detection signal is obtained for each segment to provide reproduced patterns. The detection results of such minutely divided segments are compared, to erase the common portions and leave minute portions existing in one pattern only.

Suppose that the correct pattern is the one shown in the middle column of the upper row in Figure 12 and the pattern shown in the left column of the upper row is a defective pattern, including three defective portions 35, 36 and 37. The reproduced patterns for each segment are then as shown in the left and middle columns of the middle row. Then after erasing common portions, the resultant detected defects are shown in the right column of the middle row.

It should be observed that in normal mask patterns there will be portions having smaller widths than the minimum pattern width in some characters or letters and bonding pads. However, a mask is determined to be defective when a minute portion is detected in one mask but not the other.

Using the minute comparison method, however, large defects may not be detected, although defects having dimensions smaller that the normal patterns are detected. Therefore a second method, the boundary comparison method may be used.

According to the boundary comparison method, the boundary of black to white or a pattern, i.e. outline, is detected, as shown in the left and central columns of the lower row in Figure 12. Taking out boundaries existing in both patterns, a defect pattern as shown in

the right column of the lower row.

Hence, the defective portions of the mask pattern can only be perfectly detected by adopting two kinds of algorithms, e.g. the minute comparison method and the boundary comparison method.

Once either of these methods has been performed, (xy) coordinates of each defective portion and the indentification information of the defective mask discriminated by such defect discriminating algorithm are stored in a cassette tape 38 shown in Fig. 2. The memory content of the cassette tape is as shown in Fig. 13, i.e. in the order of kind of mask, defect number (D1, D2, D3), identification of the defective mask (M1L, M2R) and the coordinates (x,y) of the defect in the mask.

Then, referring to Fig. 4, the signals stored in the parallel-out memories 58A and 58B are read into the logic circuit 59A and 59B of the next stage and the presence and absence of any minute portions or boundaries is detected.

Now, description will be made of the minute pattern comparison method in greater detail. Referring to Fig. 6, the arrangement of the read-out bits of the parallel-out memories 58A and 58B corresponding to the masks 13A and 13B will be described. When a mask pattern 61 of the minimum pattern width of 5$\mu$m is picked up in the photodiode array 23A, the mask pattern 61 allows the converted signals to be generated only for 4 $\mu$m (in the least case) through the photodiodes. When the converted signal is binary-coded, this corresponds to four bits. Therefore, any pattern of three or less bits has a large possibility of being defective. Thus, the bit structural read out from the parallel-out memories 58A and 58B should be five bits; central three bits and each end one bit.

Further, in the case of reading only such five bits disposed on a line, when there exists a protruding or denting portion 63 in the edge portion of a normal pattern 62 due to the quantization error as in Fig. 7a, there is a danger that this edge portion 63 may be detected to be defective. To avoid such faulty detection, the bits disposed on the both sides of the end bits are read out simultaneously as shown in Fig. 7b. Then, there exist no danger of detecting this edge portion 63 as defective, as seen from Fig. 73. The criteria for discriminating a defective portion are as follows:

all the bits $A_1$, $A_2$, $A_3$, $A_4$, $A_5$ and $A_6$ are "0" and at least one of the bits $C_1$, $C_2$ and $C_3$ is "1"; or

all the bits $A_1$, $A_2$, $A_3$, $A_4$, $A_5$ and $A_6$ are "1" and at least one of the bits $C_1$, $C_2$ and $C_3$ is "0".

Further, the present inventors have found that there is some danger that a normal pattern may be discriminated as defective if the reading bit structures as shown in Figs. 8a to 8d are applied similarly to the masks 13A and 13B when there exists a normal pattern, e.g. narrower that the minimum pattern width, as described above due to the error caused in the binary coding. As a result of various examinations and analyses for avoiding such faulty discriminations, it has been found that such a possibility may be eliminated by adopting different bit structures for the parallel-out memories 58A and 58B. This will be described in detail hereinbelow.

When there exists a pattern, e.g. of 4 $\mu$m, less that the minimum pattern width in each of the patterns 13A and 13B as shown in Figs. 8a and 8b, these patterns may by chance be coded to have different widths, i.e. three bits and five bits, by the photodiode arrays 23A and 23B. Now, in the case that the pattern of Fig. 8a is binary-coded to be three bits and that of Fig. 8b to be five bits, the binary signals read out from the respective parallel-out memories 58A and 58B are as shown in Figs. 8c and 8d, respectively. Then, the mask 13A is detected to have a ninute portion but the mask 13B to have no minute portions. These detection results are compared in a defect discriminating circuit 60 and the mask 13A will be erroneously discriminated to have a defect. For avoiding such erroneous discrimination, the bit structure read out from the parallel-out memory 58B for the mask 13B may be arranged to have five bits in the central portion as shown in Fig. 8e. Namely, the binary signals read out from the parallel-out memory 58B for the mask 13B become as shown in Fig. 8e and are detected to have a minute portion. As a result, the two masks coincide to each other to have a minute portion in the defect discriminating circuit 60 and this minute portion is discriminated not to be a defect.

The present inventors have also attempted various investigations and examinations to provide highly reliable defect discrimination in the consideration of the case where the bit structure of the parallel-out memory 58A for the mask 13A has three bits in the central portion as shown in Fig. 8a and that of the parallel-out memory 58B for the mask 13B has five bits in the central portion as shown in Fig. 8e and discrimination is carried out on the data from these memories only. Namely, in such an arrangement, the discrimination criteria for detecting a minute portion or boundary are as shown in Table I.

TABLE I

Conditions for detecting minute portion

| Mask | Bit structure of parallel-out memory | Criteria for detecting minute portion |
|---|---|---|
| 13A | $A_1$ $A_4$<br>$A_2$ $C_1$ $C_2$ $C_3$ $A_5$<br>$A_3$ $A_6$ | $A_1$ to $A_6$: all "0" (or "1"), and<br>$C_1$ to $C_3$: at least one "1" (or "0") |
| 13B | $B_1$ $B_4$<br>$B_2$ $C_1$ $C_2$ $C_3$ $C_4$ $C_5$ $B_5$<br>$B_3$ $B_6$ | $B_1$ to $B_6$: all "0" (or "1"), and<br>$C_1$ to $C_5$: at least one "1" (or "0") |

The discrimination criteria in the defect discriminating circuit 60 in this case will become as shown in Table II.

TABLE II

Discrimination Criteria

| Case | Detection result for mask 13A | Detection result for mask 13B | Discrimination |
|---|---|---|---|
| I | 0 | 0 | 0 |
| II | 0 | 1 | 0 |
| III | 1 | 0 | 1 |
| IV | 1 | 1 | 0 |

0: absence of minute portion.

1: existence of minute portion.

Thus, for example, when there exist no defective minute portions in the mask 13A but a defective minute portion 65 in the mask 13B as shown in Figs. 9a and 9b, the binary signals from the parallel-out memory 58A generate a detection result of absence of any minute portion and those from the parallel-out memory 58B a detection result of existence of a minute portion. For comparing these detection results in the defect discriminating circuit 60, if the criteria of Table II are adopted, the result is that there is no defective portion while there exists a defective portion in the mask 13B. Such over-looking of defective portions may be avoided by arranging the bit structures of the parallel-out memories 58A and 58B for the masks 13A and 13B as shown in Figs. 10a and 10b. When the bit signals from such parallel-out memories are read out and subjected to defect discrimination under the criteria of Tables III and IV, the minute portion in the mask 13B can be detected as a defective portion.

TABLE III

Conditions for detecting minute portion

| Mask | Bit structure of parallel-out memory | Conditions for detecting minute portion |
|---|---|---|
| 13A | $A_1$ $A_4$<br>$A_2$ $C_1$ $C_2$ $C_3$ $C_4$ $C_5$ $A_5$<br>$A_3$ $A_6$ | $A_1$ to $A_6$: all "0" (or "1"), and<br>$C_1$ to $C_5$: at least one "1", (or "0") |
| 13B | $B_1$ $B_4$<br>$B_2$ $C_1$ $C_2$ $C_3$ $B_5$<br>$B_3$ $B_6$ | $B_1$ to $B_6$: all "0" (or "1"), and<br>$C_1$ to $C_3$: at least one "1" (or "0") |

TABLE IV

Discrimination Criteria

| Case | Detection result for mask 13A | Detection result for mask 13B | Discrimination |
|---|---|---|---|
| I | 0 | 0 | 0 |
| II | 0 | 1 | 1 |
| III | 1 | 0 | 0 |
| IV | 1 | 1 | 0 |

0: absence of minute portion

1: existence of minute portion

It is impossible to completely eliminate the relative positional displacements of a pair of mask patterns due to the size errors in the masks, yawing in the translation of the xy-stage during the scanning in x- and y-directions, etc. and there exist super-position errors to some extent. In this embodiment, relative displacements of the contents in the parallel-out memories 58A and 58B up to three bits (2 $\mu$m for the relative positioning error and 1 bit for the quantization error) are tolerated. Then, the existence of a minute portion is detected in all the combinations of the bit arrangements allowing the relative shifts up to three bits in the vertical direction on the drawing and up to two bits in the horizontal direction (the quantization error one bit has already been considered in the horizontal direction as shown in Figs. 9b and 10a.

Description has been made of the case where the read-out bits of the parallel-out memories 58A and 58B are aligned in the transverse direction hereinabove. In practice, they are aligned in the transverse direction and in the longitudinal direction and minute portions are detected as described above. The results of the detection are supplied to the defect discriminating circuit 60 to perform discrimination. Fig. 11 is a block diagram of this detection and discrimination system.

Next description will be made of the boundary comparison method in greater detail. This method becomes similar to the minute pattern comparison method after the recognition of the boundary and the description will be made of the recognition of the boundary. The boundary is defined as the group of points at which the pattern changes from black (white) to white (black). This change can be known from the change

in the succeeding bits ("1" to "0" or "0" to "1") as shown in Fig. 15a. Simple detection of the change in the bit will lead to mis-discrimination of irregularities due to the quantization error as boundaries. To avoid such mis-discrimination and enable the detection of slanted boundaries, the detection bit structure is arranged as shown in Fig. 15C. The conditions for detecting a boundary in Fig. 15C are as follows:

$A_1$, $A_2$, $A_3$ and $A_4$ are all "0" and $A_5$, $A_6$, $A_7$ and $A_8$ are all "1", or $A_1$, $A_2$, $A_3$ and $A_4$ are all "1" and $A_5$, $A_6$, $A_7$ and $A_8$ are all "0".

When the bit structure of Fig. 15c is adopted similarly for the masks 13A and 13B, there is a danger of misdiscriminating a normal pattern as a defective one due to the quantization error as shown in Figs. 16a and 16b. Namely, the case of Fig. 16a generates a result that a boundary exists and that of Fig. 16b another result that there is no boundary. Such erroneous detection can be prevented by the bit structure of Fig. 16c. Further procedures are similar to those of the minute portion comparison method.

Next, the correction of defective portions will be described hereinbelow. First, a cassette tape 38 is loaded in the read-out control circuit 4 and the mask having a defective portion and the position of the defective portion in the mask are read out. Then, the defective mask 13 as thus identified is mounted on a platform or stage 39 of the exposure device 3. Here, the mask surface to be corrected is preliminarily coated with a photoresist layer and dried.

The exposure device will be described briefly. The exposure device 3 comprises a carrier 40, a stage 39 disposed on this carrier 40, the movement of which is controlled by an x-scanning motor 41 and a y-scanning motor 42, and having a linear encoder 45 for determining the position, and an optical system mounted above this stage 39 through a column 46 extending from the carrier 40 and including an objective lens systems 47, mirror cylinder 48, an eyepiece lens system 49, a slit mechanism 50 having a slit disposed in the upper part of the mirror cylinder 48, a slit driving motor 51 for adjusting the slit width, a shutter mechanism 52 having a shutter for opening a light path momentarily and a light source 53 including an ultra high pressure mercury lamp. The movements of these respective parts are automatically controlled by the read-out control device 4. Namely, the stage 39 is moved to bring a defective portion in the mask 13 precisely beneath the objective lens 47 in accordance with the information read out from the cassette tape 38. Then, the slit drive motor 51 is controlled by the information from the cassette tape 38 to determine the slit width in accordance with the size of the defective portion. Then, the shutter is actuated to sensitize the photoresist layer on the defective portion. Here, the slit width can also be adjusted manually by an operator in accordance with the size of the defective portion.

In this way, the exposure device 3 successively exposes a photoresist film on the defective portions in a mask pattern under control of the information stored in the cassette tape 38.

When the exposure for one photomask is finished, the exposed photomask is subjected to an etching treatment in the etching device 5 as shown in Fig. 2 to remove the sensitized portions of the photoresist film.

When the defective portions are excess regions outside the normal pattern, as the defective portions 35 and 37 shown in Fig. 12, the photomask is successively subjected to another etching treatment using the non-sensitized photoresist layer remaining on the photomask as an etching mask to remove such defective portions 35 and 37. In such a case, the photoresist layer is removed from the photomask thereafter to provide a mask having a normal pattern.

When the defective portions are inside the normal pattern as the defective portion 36 in Fig. 12, it means that there is no chromium film on the glass substrate where such a film should be, and hence an additional chromium layer is vacuum-deposited on the glass plate in a vacuum deposition apparatus (not shown) utilizing the photoresist layer deposited on the pattern except the defective portion 36 as a mask. Then, the photoresist layer on the mask is removed by etching to provide a normal pattern.

When there exist two kinds of defective portion in one mask, i.e. those portions to be removed and those portions to be additionally deposited, two kinds of defect correcting process should be performed successively. In practice, the defect correction of depositing a new metal layer is not suited for fine patterns and may be adequately adopted for such masks as the master reticule in which the pattern is formed ten times as large as the actual one.

According to the above embodiments, defective portions and the positions thereof in a pair of masks can be detected accurately without mis-discrimination by comparing the pair of masks. In this embodiment, defective portions having a width larger than 1 $\mu$m or a diameter larger than 2 $\mu$m can be reliably detected without failure based on the accuracies of the mask inspection unit.

Further, in this embodiment, defective portions and the positions thereof are recorded in a cassette tape and the defect

correction processes are carried out using the information stored in the tape. Thus, the correction is reliable and the operation efficiency is greatly enhanced due to the automated operations.

It is to be noted that this invention is not limited to the above embodiment. For example, the information recorded in the cassette tape may be that for a single mask but not for successive masks. The recording medium may be any one such as a disk, core memory, etc. other than a magnetic tape. A random access memory may also be used to store and read out the information for correction of defective masks.

In a modification embodiment, defective portions may be removed by the use of a laser beam. Namely, as shown in Fig. 14, a laser oscillator 67, e.g. an Argon laser oscillator, is used to irradiate a laser beam directly on the detected defective portions in a mask 13. The irradiation spot of the laser beam is controlled by the information stored in a cassette tape as described above. In the figure, numerals 68 and 69 denote prisms for scanning the laser beam. The laser beam can be scanned in a certain area by rotating these prisms. Numerals 70 and 71 are condenser lenses for condensing the laser beam and a stage for mounting the mask 13. The details of this technique are disclosed in our German Offenlegungsschrift No. 2638474 published on 10th March 1977 and corresponding to British Patent Specification No. 1554296.

Minute defects in masks can be reliably detected and corrected as has been described above. Further, since the inspection and the correction of defective portions are mostly automated, the operation efficiency is greatly improved.

Furthermore since defective portions in masks are reliably detected in the detection process and identified from the information obtained in the detection in the correction processes, the detected defective portions can be reliably removed to greatly improve the yield.

Attention is drawn to Britich Patent Application No. 21235/78 (published under No. 1574512), which was divided from this application, in which is disclosed a video signal processing device for processing an electrical video signal of mask pattern into a binary coded form including: converter means for converting an image of the pattern of said mask into the electrical video signal; a threshold voltage generator for generating a first, a second and a third threshold voltage corresponding to a bright, level, a normal or average level and a dark level of said electrical video signal respectively; a first circuit means for comparing said electrical video signal with said first threshold voltage to generate first signals dependent on said first threshold voltage; a second circuit means for comparing said electrical video signal with said second threshold voltage to generate second signals dependent on said second threshold voltage; a third circuit means for comparing said electrical video signal with said third threshold voltage to generate third signals dependent on said third threshold voltage; a first parallel-out shift register, an input of which is coupled to said first circuit means, for storing a plurality of said first signals from said first circuit means and for shifting said first signals from the one end bit position at said input to the other end bit position through the central bit position thereof successively, said first parallel-out shift register outputting the plurality of said first signals in parallel from said central bit position and from the preceding and succeeding bit positions with respect to said central bit position; a second parallel-out shift register, an input of which is coupled to said second circuit means, for storing a plurality of said second signals from said second circuit means and for shifting said second signals from the one end bit position at said input to the other end bit position through the central bit position thereof successively, said second parallel-out shift register outputting the plurality of said second signals in parallel from said central bit position and from the preceding and succeeding bit positions with respect to said central bit position; a third parallel-out shift register, an input of which is coupled to said third circuit means, for storing a plurality of said third signals from said third circuit means and for shifting said third signals from the one end bit position at said input to the other end bit position through the central bit position thereof successively, said third parallel-out shift register outputting the plurality of said third signals in parallel from said central bit position and from the preceding and succeeding bit positions with respect to said central bit position; a first gate means having an input to receive said first signals from said first parallel-out shift register and a control terminal to receive a first selection signal; a second gate means having an input to receive said second signals from said second parallel-out shift register and a control terminal to receive a second selection signal; a third gate means having an input to receive said third signals from said third parallel-out shift register and a control terminal to receive a third selection signal; and gate selection means for receiving all signals from said preceding, said central and said succeeding bit position of said first, second and third parallel-out shift registers and for detecting whether said signals from said preceding, said central and said

succeeding bit position of said first parallel-out shift register are all at the same level, whether said signals from said preceding, said central and said succeeding bit position of said second parallel-out shift register are all at the same level and whether said signals from said preceding, said central and said succeeding bit position of said third parallel-out shift register are all at the same level to generate said first, said second and said third selection signal; one of said first, second or third gate means being caused to transmit said first, said second or said third signal respectively as the binary coded form of said mask pattern in response to said first, second or said third selection signal.

WHAT WE CLAIM IS:—

1. A method of inspecting masks used in forming a desired oxide pattern or a desired wiring pattern on a semiconductor wafer and wherein each mask is formed from a layer of an opaque material deposited in a predetermined pattern of a surface of a transparent substrate, a portion of the layer of the opaque material being designed to have a predetermined minimum pattern width; the method comprising the steps of;

mounting a pair of similar masks on a mounting stage;

converting images of the patterns of the masks into electrical video signals respectively;

converting said electrical video signals into binary signals on the basis of at least one reference threshold value;

storing a plurality of bits of said binary signals corresponding to said minimum pattern width;

comparing the central bit of stored binary signals with the each end bit of the stored binary signals so as to detect a minute portion (as hereinbefore defined); and

detecting defects in at least one of the masks by comparing the results of detecting minute portions in said two patterns so as to cancel signals representing the common minute portions and leave a signal representing minute portions existing in one only of the two patterns.

2. A method of inspecting masks according to claim 1, in which binary signals corresponding to boundaries in the patterns are obtained from the changes in successive bits of the stored binary signals and the results of detecting the binary signals corresponding to boundaries in said two patterns are compared so as to cancel signals representing the common boundary portions and leave a signal representing the boundary portions existing in one only of the two patterns.

3. A method of inspecting masks according to claim 1 or claim 2, wherein a plurality of bits of the binary signals are converted from the image of a first of said two patterns and plurality of bits of the binary signals are converted from the image of the second of said two patterns respectively, wherein the number of bits of binary signals converted from the image of the first pattern corresponds to the quantization of the minimum patterns width and the number of bits of the binary signals converted from the image of the second pattern is larger than that of the binary signals converted from the image of the first pattern and the central bit is compared with each end bit in the stored binary signals converted from the image of the first pattern and also the central bit is compared with each end bit in the stored binary signals converted from the image of the second pattern and the detection of the minute portions in first of the two patterns is carried out according to Table II in the specification, and wherein the number of bits of the binary signals converted from the image of the second pattern corrsponds to the quantization of the minimum pattern width and the number of bits of the binary signals converted from the image of the first is larger than that of the binary signals converted from the second pattern and the central bit is compared with each end bit in the stored binary signals converted from the image of the first pattern and also the central bit is compared with each end bit in the stored binary signals converted from the image of the second pattern and the detection of minute portions in the second patterns is carried out according to Table IV in the specification.

4. A method of inspecting masks according to any one of the preceding claims, further including the steps of;

detecting which mask has the minute portion existing in one of the two patterns and the position of this minute portion;

recording the results of the detection in a memory means;

reading out which mask has the minute portion existing in one of the two patterns and the position of this portion; and

correcting the minute portion existing in one of the two masks.

5. A method of inspecting and correcting masks according to claim 4, wherein said correcting step includes the steps of;

coating a photosensitive material onto the whole of one principle surface of the mask detected to have the minute portion existing in one of the two patterns;

sensitizing the photosensitive material corresponding to the defect or corresponding to the material except the defect based on the information obtained from the inspection of said pattern and read out from said memory means;

removing the photosensitive material on

succeeding bit position of said first parallel-out shift register are all at the same level, whether said signals from said preceding, said central and said succeeding bit position of said second parallel-out shift register are all at the same level and whether said signals from said preceding, said central and said succeeding bit position of said third parallel-out shift register are all at the same level to generate said first, said second and said third selection signal; one of said first, second or third gate means being caused to transmit said first, said second or said third signal respectively as the binary coded form of said mask pattern in response to said first, second or said third selection signal.

WHAT WE CLAIM IS:—

1. A method of inspecting masks used in forming a desired oxide pattern or a desired wiring pattern on a semiconductor wafer and wherein each mask is formed from a layer of an opaque material deposited in a predetermined pattern of a surface of a transparent substrate, a portion of the layer of the opaque material being designed to have a predetermined minimum pattern width; the method comprising the steps of;

mounting a pair of similar masks on a mounting stage;

converting images of the patterns of the masks into electrical video signals respectively;

converting said electrical video signals into binary signals on the basis of at least one reference threshold value;

storing a plurality of bits of said binary signals corresponding to said minimum pattern width;

comparing the central bit of stored binary signals with the each end bit of the stored binary signals so as to detect a minute portion (as hereinbefore defined); and

detecting defects in at least one of the masks by comparing the results of detecting minute portions in said two patterns so as to cancel signals representing the common minute portions and leave a signal representing minute portions existing in one only of the two patterns.

2. A method of inspecting masks according to claim 1, in which binary signals corresponding to boundaries in the patterns are obtained from the changes in successive bits of the stored binary signals and the results of detecting the binary signals corresponding to boundaries in said two patterns are compared so as to cancel signals representing the common boundary portions and leave a signal representing the boundary portions existing in one only of the two patterns.

3. A method of inspecting masks according to claim 1 or claim 2, wherein a plurality of bits of the binary signals are converted from the image of a first of said two patterns and plurality of bits of the binary signals are converted from the image of the second of said two patterns respectively, wherein the number of bits of binary signals converted from the image of the first pattern corresponds to the quantization of the minimum patterns width and the number of bits of the binary signals converted from the image of the second pattern is larger than that of the binary signals converted from the image of the first pattern and the central bit is compared with each end bit in the stored binary signals converted from the image of the first pattern and also the central bit is compared with each end bit in the stored binary signals converted from the image of the second pattern and the detection of the minute portions in first of the two patterns is carried out according to Table II in the specification, and wherein the number of bits of the binary signals converted from the image of the second pattern corrsponds to the quantization of the minimum pattern width and the number of bits of the binary signals converted from the image of the first is larger than that of the binary signals converted from the second pattern and the central bit is compared with each end bit in the stored binary signals converted from the image of the first pattern and also the central bit is compared with each end bit in the stored binary signals converted from the image of the second pattern and the detection of minute portions in the second patterns is carried out according to Table IV in the specification.

4. A method of inspecting masks according to any one of the preceding claims, further including the steps of;

detecting which mask has the minute portion existing in one of the two patterns and the position of this minute portion;

recording the results of the detection in a memory means;

reading out which mask has the minute portion existing in one of the two patterns and the position of this portion; and

correcting the minute portion existing in one of the two masks.

5. A method of inspecting and correcting masks according to claim 4, wherein said correcting step includes the steps of;

coating a photosensitive material onto the whole of one principle surface of the mask detected to have the minute portion existing in one of the two patterns;

sensitizing the photosensitive material corresponding to the defect or corresponding to the material except the defect based on the information obtained from the inspection of said pattern and read out from said memory means;

removing the photosensitive material on

said defect by etching; and

depositing a new opaque film on said defect region of the pattern using the remaining photosensitive material as a mask or removing the opaque material deposited on the defect region, thereby correcting defect portions in the mask.

6. A method of inspecting and correcting masks according to claim 5, wherein the opaque material being in the excess region outside of the normal pattern is removed by irradiation with a laser beam.

7. An apparatus for inspecting the pattern of a mask of the type used in forming a desired oxide pattern or a desired wiring pattern on a semiconductor wafer and of the type formed from a layer of opaque material deposited in a predetermined pattern on a surface of a transparent substrate a portion of the layer of opaque material being designed to have a predetermined minimum pattern width in order to detect a defective portion therein including;

means for mounting a pair of masks in a predetermined positional relation to each other and for shifting said pair of masks in a plane by the same amount;

a pair of opto-electrical converter means located in a predetermined positional relation with said mask mounting means for converting received images of the mask patterns into electrical video signals;

optical means for directing light on to said pair of masks and for focusing the images of said pair of patterns on said pair of opto-electrical converter means;

a pair of binary -coding means for transforming the electrical video signals from said converter means into respective binary signals;

a pair of memory circuits for storing a respective plurality of bits of the binary signals corresponding to the minimum pattern width and

a detecting circuit which compares the central bit with each end bit in each plurality of stored binary signals so as to detect a minute portion (as hereinbefore defined), and which compares the results of detection of the minute portions in the two patterns so as to cancel signals representing the common minute portions and leave minute portions existing in one only of the two patterns.

8. An apparatus according to claim 7, in which the detecting circuit further compares the boundaries of the two patterns by comparing binary signals corresponding to boundaries in the patterns, obtained from the changes in successive bits in the binary signals converted from the two patterns so as to cancel signals representing the common minute portions leave the boundary portions existing in one only of the two patterns.

9. An apparatus according to claim 8, further including memory means for storing and reproducing the information of the detecting minute portions from the detecting circuit and exposure means responsive to the information of detected defective portions reproduced from said memory means for selectively exposing a part of a photosensitive film coated on said patterns.

10. A method of inspecting masks substantially as herein described with reference to the accompanying drawings.

11. An apparatus for inspecting masks substantially as herein described with refernce to and as illustrated in the accompanying drawings.

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Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1980.
Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.