ABSTRACT

PIPELINED FAST FOURIER TRANSFORM PROCESSOR

A pipelined Fast Fourier Transform Processor includes, besides a memory arrangement, a cascade of a first arithmetic unit, a scratch memory and a second arithmetic unit. One of both arithmetic units can only perform at least one type of butterfly Fast Fourier Transform arithmetic calculations, whereas the other one can perform, besides this at least one type of butterfly Fast Fourier Transform arithmetic calculations , at least one second type of butterfly Fast Fourier Transform arithmetic calculations. This architecture optimises both timing as well as circuit restrictions.

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