SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide degradation resistance for metals in contact with fluorine-containing insulator materials.

It is another object of the present invention to provide corrosion resistance for aluminum lines in contact with oxide insulator lines containing fluorine.

It is yet another objective of this invention to prevent fluorine poisoning of metals used in IC metallization schemes to prevent undesired via resistance growth and to enhance the contact between a metallization layer and the metal in a via plug.

These and other objectives are achieved in the present invention by providing a fluorine-free barrier layer between an insulator material containing fluorine and a metal to effectively restrict diffusion of fluorine from the insulator material into the metal thereby preventing metal degradation.

According to a first embodiment of the invention, there is provided a method of improving the resistance of a metal against degradation from exposure to fluorine:

providing an insulator material containing fluorine;

forming a fluorine-free barrier layer on said insulator material; and

forming metal on said fluorine-free barrier layer.

According to a second embodiment of the invention, there is provided a method of improving degradation resistance of a metal, comprising the steps of:

providing an insulator film containing fluorine;

depositing a fluorine-free barrier layer on said insulator film; and

forming a pattern of metal lines on top of said fluorine-free barrier layer.

According to a third embodiment of the invention, there is provided a method of improving degradation resistance of a metal, comprising the steps of:

providing an insulator film containing fluorine having a surface region;

removing fluorine from said surface region of said insulator film to form a fluorine-free barrier layer on said insulator film; and

forming a pattern of metal lines on top of said fluorine-free barrier layer.

According to a fourth embodiment of the invention, there is provided an integrated circuit structure, comprising:

a substrate;

patterned metallization formed on said substrate;

a fluorine-containing insulator layer formed on said substrate and adjacent said patterned metallization; and

a fluorine-free barrier layer between said fluorine-containing insulator layer and said patterned metallization.

According to a fifth embodiment of the invention, there is provided an integrated circuit structure, comprising:

a substrate;

patterned metallization formed on said substrate;

a fluorine-containing insulator layer formed on said substrate and adjacent said patterned metallization;

a first fluorine-free barrier layer between said fluorine-containing insulator layer and said patterned metallization; and

a second fluorine-free barrier layer formed on top of said fluorine containing insulator layer.

For purposes of the present invention, the terminology "degradation", as used in connection with metal contact and metal-based conductors of electricity, encompasses "corrosion" or "poisoning" of a metal. "Corrosion" of a metal line or metal contact by exposure to fluorine means formation of a metal fluoride compound from fluorine and the metal via chemical reaction. "Poisoning" of a metal by exposure to fluorine means physical infiltration of the metal by fluorine as a contaminant in an amount adequate to increase the contact resistance of the

CLAIMS

We claim:

1. A method of improving the resistance of a metal against degradation from exposure to fluorine:

providing an insulator material containing fluorine;

forming a fluorine-free barrier layer on said insulator material; and

forming metal on said fluorine-free barrier layer.

2. A method of improving degradation resistance of a metal , comprising the steps of:

providing an insulator film containing fluorine;

depositing a fluorine-free barrier layer on said insulator film; and

forming a pattern of metal lines on top of said fluorine-free barrier layer.

3. The method of claim 2, wherein said fluorine-free barrier layer is a material devoid of fluorine selected from the group consisting of silicon, silicon dioxide, silicon nitride, and carbon.

4. The method of claim 2, wherein said step of depositing said fluorine-free barrier layer comprises a deposition process selected from the group consisting of PECVD, PVD, HDPCVD, and LPCVD.

5. The method of claim 2, wherein said insulator film is an oxide insulator film.

6. The method of claim 2, wherein said insulator film is SiO_zF_{2-z} where $0 < z < 2$.

7. The method of claim 2, wherein said metal lines comprise metal material selected from the group consisting of Al, Al-Si, Al-Cu, Al-Si-Cu, Cu, Cu-Sn, Cu-Si, Au, Au-Zn, Au-Ge, Ni, Cr, $CrSi_2$, Ge, Mo, $MoSi_2$, Pd, $PdSi_2$, Pt, PtSi, Ta, $TaSi_2$, Ti, TiN, Ti-Pt, Ti-W, $TiSi_2$, W, WSi_2, WN, and $ZrSi_2$.

8. The method of claim 2, wherein said metal lines comprise metal material selected from the group consisting of an aluminum-containing material, a titanium-containing material, and a copper-containing material.

9. The method of claim 2, wherein said metal lines are an aluminum-containing material.

10. The method of claim 2, wherein said fluorine-free barrier layer has a thickness ranging from 1 nm to 300 nm.

11. A method of improving degradation resistance of a metal, comprising the steps of:

providing an insulator film containing fluorine having a surface region;

removing fluorine from said surface region of said insulator film to form a fluorine-free barrier layer on said insulator film; and

forming a pattern of metal lines on top of said fluorine-free barrier layer.

12. The method of claim 11, wherein said removing of fluorine from said surface region is accomplished by exposing said surface region to a hydrogen annealing.

13. The method of claim 11, wherein said removing of fluorine from said surface region is accomplished by exposing said surface region to an ozone plasma.

14. The method of claim 11, wherein said fluorine-free barrier layer has a thickness ranging from 1 nm to 300 nm.

15. An integrated circuit structure, comprising:

a substrate;

patterned metallization formed on said substrate;

a fluorine-containing insulator layer formed on said substrate and adjacent said patterned metallization; and

a fluorine-free barrier layer between said fluorine-containing insulator layer and said patterned metallization.

16. The integrated circuit structure of claim 15 comprising an opening formed in said fluorine containing insulator layer, and wherein said fluorine-free barrier layer is positioned on sidewalls of said opening in said fluorine containing insulator layer.

17. The integrated circuit structure of claim 16 wherein said opening is selected from the group consisting of a via or trench.

18. An integrated circuit structure, comprising:

a substrate;

patterned metallization formed on said substrate;

a fluorine-containing insulator layer formed on said substrate and adjacent said patterned metallization;

a first fluorine-free barrier layer between said fluorine-containing insulator layer and said patterned metallization; and

a second fluorine-free barrier layer formed on top of said fluorine-containing insulator layer.

19. The integrated circuit structure of claim 18, wherein a metal-filled via opening is present through said second fluorine barrier material, said insulator layer, and said first fluorine-free barrier layer, wherein the metal-filled via opening contacts said patterned metallization.

20. The integrated circuit structure of claim 19, wherein a second level of metallization is formed on top of said second fluorine-free barrier layer in contact with said metal-filled via opening.