WHAT IS CLAIMED IS:

1. A storage device comprising:

a first memory device including a plurality of first memory cells;

a second memory device including a plurality of second memory cells having a same type as the plurality of first memory cells; and

a controller configured to communicate with the first memory device through a first memory interface and to communicate with the second memory device through a second memory interface having an operating speed higher than an operating speed of the first memory interface,

wherein the first memory device includes a plurality of first data signal pins connected with the first memory interface, the plurality of first data signal pins being arranged in an edge area of the first memory device,

the second memory device includes a plurality of second data signal pins connected with the second memory interface, the plurality of second data signal pins being arranged in a center area of the second memory device, and

a number of the second data signal pins is more than a number of the first data signal pins, and

wherein the second memory device includes a multiply and accumulate (MAC) engine configured to:

perform a MAC operation on data provided from the controller through the second memory interface and weight information stored in the plurality of second memory cells, and

output a result of the MAC operation through the second memory interface.

2. The storage device of claim 1, wherein each of the plurality of first memory cells and the plurality of second memory cells is a NAND flash memory cell.

3. The storage device of claim 1 or claim 2, wherein:

the first memory device operates in response to a first command latch enable signal, a first address latch enable signal, a first write enable signal, a first read enable signal, and a plurality of first data signals provided through the first memory interface,

the second memory device operates in response to a second command latch enable signal, a second address latch enable signal, a second write enable signal, a second read enable signal, and a plurality of second data signals provided through the second memory interface, and

a number of the plurality of second data signals is more than a number of the plurality of first data signals.

4. The storage device of any one of claims 1 to 3, wherein:

the plurality of first memory cells of the first memory device are divided into a plurality of first planes,

the plurality of second memory cells of the second memory device are divided into a plurality of second planes, and

a number of the second planes is more than a number of the first planes.

5. The storage device of any one of claims 1 to 4, wherein a size of data exchanged through the second memory interface per unit time is greater than a size of data exchanged through the first memory interface per unit time.

6. The storage device of any one of claims 1 to 5, wherein the controller includes:

a first memory interface circuit configured to communicate with the first memory device through the first memory interface;

a second memory interface circuit configured to communicate with the second memory device through the second memory interface;

a first processor configured to control the first memory interface circuit to perform an access operation on the first memory device; and

a second processor configured to control the second memory interface circuit to perform an access operation on the second memory device.

7. The storage device of claim 6, wherein:

the first processor is further configured to store first user data provided from an external device in the first memory device or to provide second user data stored in the first memory device to the external device, and

the second processor is further configured to perform a special operation on special data provided from the external device based on weight information stored in the second memory device and to provide a result of the special operation to the external device.

8. The storage device of any one of claims 1 to 7, further comprising:

a third memory device including a plurality of third memory cells having a same type as the plurality of first memory cells and configured to communicate with the controller through the first memory interface, wherein:

the first memory device communicates with the controller through a first channel of the first memory interface, and

the third memory device communicates with the controller through a second channel of the first memory interface.

9. The storage device of any one of claims 1 to 7, further comprising a third memory device including a plurality of third memory cells having a same type as the plurality of first memory cells and configured to communicate with the controller through a third memory interface.

10. A storage device comprising:

a first controller configured to communicate with an external device through a host interface;

a first memory device including a plurality of first memory cells, and configured to communicate with the first controller through a first channel of a first memory interface;

a second memory device including a plurality of second memory cells having a same type as the plurality of first memory cells; and

a second controller configured to communicate with the first controller through a second channel of the first memory interface, wherein the second controller communicates with the second memory device through a second memory interface,

wherein the second memory device includes a multiply and accumulate (MAC) engine configured to:

perform a MAC operation on data provided from the second controller through the second memory interface and weight information stored in the plurality of second memory cells, and

output a result of the MAC operation through the second memory interface.

11. The storage device of claim 10, wherein each of the plurality of first memory cells and the plurality of second memory cells is a NAND flash memory cell.

12. The storage device of claim 10 or claim 11, wherein:

the first memory device operates in response to a first command latch enable signal, a first address latch enable signal, a first write enable signal, a first read enable signal, and a plurality of first data signals provided through the first memory interface,

the second memory device operates in response to a second command latch enable signal, a second address latch enable signal, a second write enable signal, a second read enable signal, and a plurality of second data signals provided through the second memory interface, and

a number of the plurality of second data signals is more than a number of the plurality of first data signals.

13. The storage device of any one of claims 10 to 12, wherein:

the first memory device includes a plurality of first data signal pins connected with the first memory interface,

the second memory device includes a plurality of second data signal pins connected with the second memory interface, and

a number of the second data signal pins is more than a number of the first data signal pins.

14. The storage device of any one of claims 10 to 13, wherein:

the plurality of first memory cells of the first memory device are divided into a plurality of first planes, and the plurality of second memory cells of the second memory device are divided into a plurality of second planes, and

a number of the second planes is more than a number of the first planes.

15. The storage device of any one of claims 10 to 14, further comprising a third memory device including a plurality of third memory cells having a same type as the plurality of first memory cells and configured to communicate with the second controller through a third memory interface.

16. A storage device comprising:

a first memory device including a plurality of first NAND flash memory cells;

a second memory device including a plurality of second NAND flash memory cells; and

a controller configured to communicate with the first memory device through a first memory interface and to communicate with the second memory device through a second memory interface having a larger input/output bandwidth than the first memory interface,

wherein the second memory device includes a multiply and accumulate (MAC) engine configured to:

perform a MAC operation on data provided from the controller through the second memory interface and weight information stored in the plurality of second NAND flash memory cells, and

output a result of the MAC operation through the second memory interface.

17. The storage device of claim 16, wherein:

the first memory device operates in response to a first command latch enable signal, a first address latch enable signal, a first write enable signal, a first read enable signal, and a plurality of first data signals provided through the first memory interface,

the second memory device operates in response to a second command latch enable signal, a second address latch enable signal, a second write enable signal, a second read enable signal, and a plurality of second data signals provided through the second memory interface, and

a number of the plurality of second data signals is more than a number of the plurality of second data signals.