

the DRAM portion is at least as large as the particular storage capacity of each partition. In certain implementations, each NAND flash chip includes multiple partitions, each partition having a particular storage capacity and the second storage capacity of the DRAM portion is either approximately equal to or approximately double the size of the particular storage capacity of each partition.

[0013] In certain implementations, the plurality of NAND flash chips are part of a module coupled to an input/output (I/O) bus, and the module further includes the DRAM portion, wherein the second storage capacity of the DRAM portion is approximately double the size of the first storage capacity of each NAND flash chip. In certain implementations, the plurality of NAND flash chips are coupled to an input/output (I/O) bus, and the DRAM portion is part of a main memory comprising DRAM. In certain implementations, the plurality of NAND flash chips and the DRAM portion are part of a module, and the second storage capacity of the DRAM portion is at least as large as double the first storage capacity of each NAND flash chip.

[0013a] According to an aspect, there is provided a memory device, comprising: a plurality of NAND flash chips, each of the plurality of NAND flash chips comprising a memory section, wherein each memory section comprises a plurality of pages, and wherein each NAND flash chip has a first storage capacity; a dynamic random access memory (DRAM) portion in data communication with the NAND flash chips, the DRAM portion having a second storage capacity that is at least as large as the first storage capacity of each of the plurality of NAND flash chips; and a controller configured to: select one of the NAND flash chips as a currently selected NAND flash chip for writing data; copy all valid pages in the currently selected NAND flash chip into the DRAM portion; and in response to a write request to a logical memory location that is mapped to a particular physical location in one of the NAND flash chips, allocate the currently selected NAND flash chip for writing to a particular page that includes the particular physical location; wherein the plurality of NAND flash chips and the DRAM portion are part of a module coupled to a memory bus, and wherein the second storage capacity of

the DRAM portion is at least as large as double the first storage capacity of each NAND flash chip.

[0013b] According to another aspect, there is provided a memory device, comprising: a plurality of NAND flash chips, each of the plurality of NAND flash chips comprising a memory section, wherein each memory section comprises a plurality of pages, and wherein each NAND flash chip has a first storage capacity; a dynamic random access memory (DRAM) portion in data communication with the NAND flash chips, the DRAM portion having a second storage capacity that is at least as large as the first storage capacity of each of the plurality of NAND flash chips; and a controller configured to: select one of the NAND flash chips as a currently selected NAND flash chip for writing data; copy all valid pages in the currently selected NAND flash chip into the DRAM portion; and in response to a write request to a logical memory location that is mapped to a particular physical location in one of the NAND flash chips, allocate the currently selected NAND flash chip for writing to a particular page that includes the particular physical location; wherein the plurality of NAND flash chips are part of a module coupled to an input/output (I/O) bus, the module further comprising the DRAM portion, wherein the second storage capacity of the DRAM portion is approximately double the size of the first storage capacity of each NAND flash chip.

[0013c] According to yet another aspect, there is provided a method comprising: selecting one of a plurality of NAND flash chips as a currently selected NAND flash chip for writing data, each of the plurality of NAND flash chips comprising a memory section, wherein each memory section comprises a plurality of pages, and wherein each NAND flash chip has a first storage capacity; copying all valid pages in the currently selected NAND flash chip into a dynamic random access memory (DRAM) portion that is in data communication with the NAND flash chips, wherein the DRAM portion has a second storage capacity that is at least as large as the first storage capacity of each of the plurality of NAND flash chips; and in response to a write request to a logical memory location that is mapped to a particular physical location in one of the NAND flash chips, allocate the currently selected NAND flash chip for writing to a particular page that

includes the particular physical location; wherein the plurality of NAND flash chips and the DRAM portion are part of a module, and wherein the second storage capacity of the DRAM portion is at least as large as double the first storage capacity of each NAND flash chip.

[0013c] According to yet another aspect, there is provided method comprising: selecting one of a plurality of NAND flash chips as a currently selected NAND flash chip for writing data, each of the plurality of NAND flash chips comprising a memory section, wherein each memory section comprises a plurality of pages, and wherein each NAND flash chip has a first storage capacity; copying all valid pages in the currently selected NAND flash chip into a dynamic random access memory (DRAM) portion that is in data communication with the NAND flash chips, wherein the DRAM portion has a second storage capacity that is at least as large as the first storage capacity of each of the plurality of NAND flash chips; and in response to a write request to a logical memory location that is mapped to a particular physical location in one of the NAND flash chips, allocate the currently selected NAND flash chip for writing to a particular page that includes the particular physical location; wherein the plurality of NAND flash chips are part of a module coupled to an input/output (I/O) bus, the module further comprising the DRAM portion, wherein the second storage capacity of the DRAM portion is approximately double the size of the first storage capacity of each NAND flash chip.

[0014] The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features and advantages of the invention will become apparent from the description, the drawings, and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1 depicts an example of a system including a memory device according to implementations of the present disclosure.

[0016] FIG. 2A depicts an example of a system including a memory device according to implementations of the present disclosure.

[0017] FIG. 2B depicts an example of a system including a memory device according to implementations of the present disclosure.

CLAIMS

1. A memory device, comprising:
 - a plurality of NAND flash chips, each of the plurality of NAND flash chips comprising a memory section, wherein each memory section comprises a plurality of pages, and wherein each NAND flash chip has a first storage capacity;
 - a dynamic random access memory (DRAM) portion in data communication with the NAND flash chips, the DRAM portion having a second storage capacity that is at least as large as the first storage capacity of each of the plurality of NAND flash chips; and
 - a controller configured to:
 - select one of the NAND flash chips as a currently selected NAND flash chip for writing data;
 - copy all valid pages in the currently selected NAND flash chip into the DRAM portion; and
 - in response to a write request to a logical memory location that is mapped to a particular physical location in one of the NAND flash chips, allocate the currently selected NAND flash chip for writing to a particular page that includes the particular physical location;
 - wherein the plurality of NAND flash chips and the DRAM portion are part of a module coupled to a memory bus, and wherein the second storage capacity of the DRAM portion is at least as large as double the first storage capacity of each NAND flash chip.
2. The memory device of claim 1, wherein the at least one controller is configured to:
 - select another one of the plurality of NAND flash chips as a queued NAND flash chip for writing data after the currently selected NAND flash chip is identified as full; and
 - copy all valid pages in the queued NAND flash chip into the DRAM portion.
3. The memory device of claim 2, wherein the another one of the plurality of NAND flash chips is selected as a queued NAND flash chip based on having the fewest number of valid pages of the plurality of NAND flash chips.

4. The memory device of claim 1, wherein the particular physical location to write data to the currently selected NAND flash chip is determined based on at least one of: (i) least accessed page and (ii) least recently used page.
5. The memory device of claim 1, wherein the memory section comprises a partition of the respective NAND flash chip, and wherein partitions allow the operation of a read in a first partition of the respective NAND flash chip during a write operation in another partition of the same respective NAND flash chip.
6. The memory device of claim 1, wherein the memory section comprises the respective constituent NAND flash chip.
7. A memory device, comprising:
 - a plurality of NAND flash chips, each of the plurality of NAND flash chips comprising a memory section, wherein each memory section comprises a plurality of pages, and wherein each NAND flash chip has a first storage capacity;
 - a dynamic random access memory (DRAM) portion in data communication with the NAND flash chips, the DRAM portion having a second storage capacity that is at least as large as the first storage capacity of each of the plurality of NAND flash chips; and
 - a controller configured to:
 - select one of the NAND flash chips as a currently selected NAND flash chip for writing data;
 - copy all valid pages in the currently selected NAND flash chip into the DRAM portion; and
 - in response to a write request to a logical memory location that is mapped to a particular physical location in one of the NAND flash chips, allocate the currently selected NAND flash chip for writing to a particular page that includes the particular physical location;
 - wherein the plurality of NAND flash chips are part of a module coupled to an input/output (I/O) bus, the module further comprising the DRAM portion, wherein the second storage capacity of the DRAM portion is approximately double the size of the first storage capacity of each NAND flash chip.

8. The memory device of claim 1, wherein the DRAM portion is part of a main memory comprising DRAM.
9. The memory device of claim 1, wherein the at least one controller is configured to:
read in to a main memory comprising DRAM a particular page from the plurality of NAND flash chips in response to a request to access the particular page stored in the plurality of NAND flash chips.
10. A method comprising:
selecting one of a plurality of NAND flash chips as a currently selected NAND flash chip for writing data, each of the plurality of NAND flash chips comprising a memory section, wherein each memory section comprises a plurality of pages, and wherein each NAND flash chip has a first storage capacity;
copying all valid pages in the currently selected NAND flash chip into a dynamic random access memory (DRAM) portion that is in data communication with the NAND flash chips, wherein the DRAM portion has a second storage capacity that is at least as large as the first storage capacity of each of the plurality of NAND flash chips; and
in response to a write request to a logical memory location that is mapped to a particular physical location in one of the NAND flash chips, allocate the currently selected NAND flash chip for writing to a particular page that includes the particular physical location;
wherein the plurality of NAND flash chips and the DRAM portion are part of a module, and wherein the second storage capacity of the DRAM portion is at least as large as double the first storage capacity of each NAND flash chip.
11. The method of claim 10, further comprising:
selecting another one of the plurality of NAND flash chips as a queued NAND flash chip for writing data after the currently selected NAND flash chip is identified as full; and
copying all valid pages in the queued NAND flash chip into the DRAM portion.

12. The method of claim 11, wherein the another one of the plurality of NAND flash chips is selected as a queued NAND flash chip based on having the fewest number of valid pages of the plurality of NAND flash chips.

13. The method of claim 10, wherein the particular physical location to write data to the currently selected NAND flash chip is determined based on at least one of: (i) least accessed page and (ii) least recently used page.

14. The method of claim 10, wherein the memory section comprises a partition of the respective NAND flash chip, and wherein partitions allow the operation of a read in a first partition of the respective NAND flash chip during a write operation in another partition of the same respective NAND flash chip.

15. The method of claim 10, wherein the memory section comprises the respective constituent NAND flash chip.

16. A method comprising:

selecting one of a plurality of NAND flash chips as a currently selected NAND flash chip for writing data, each of the plurality of NAND flash chips comprising a memory section, wherein each memory section comprises a plurality of pages, and wherein each NAND flash chip has a first storage capacity;

copying all valid pages in the currently selected NAND flash chip into a dynamic random access memory (DRAM) portion that is in data communication with the NAND flash chips, wherein the DRAM portion has a second storage capacity that is at least as large as the first storage capacity of each of the plurality of NAND flash chips; and

in response to a write request to a logical memory location that is mapped to a particular physical location in one of the NAND flash chips, allocate the currently selected NAND flash chip for writing to a particular page that includes the particular physical location;

wherein the plurality of NAND flash chips are part of a module coupled to an input/output (I/O) bus, the module further comprising the DRAM portion, wherein the second

storage capacity of the DRAM portion is approximately double the size of the first storage capacity of each NAND flash chip.

17. The memory device of claim 10, wherein the DRAM portion is part of a main memory comprising DRAM.

18. The method of claim 10, further comprising:

reading in to a main memory comprising DRAM a particular page from the plurality of NAND flash chips in response to a request to access the particular page stored in the plurality of NAND flash chips.