performed and accordingly, the loop counting value LC is reduced in operation S36 and a program counting value instructs an instruction corresponding to the target included in the loop instruction in operation S37. Accordingly, when the command/address instructing the next operation to be processed is received, the instruction corresponding to the target may be executed without executing the loop instruction.

[00121] On the other hand, when it is determined that the loop counting value LC corresponds to 0, it represents that the loop has executed the determined number of times. Accordingly, the program counting value may change so as to instruct a next instruction in operation S38.

[00122] FIGS. 15A and 15B are views illustrating a basic block and an operation example of instructions that perform a loop (execute a loop instruction) according to exemplary embodiments of the inventive concept.

[00123] Referring to FIG. 15A, a basic block (e.g., a code block) includes one or more instructions. For example, in the basic block, the first instruction Inst0 performing a first function Function A, the second instruction Inst1 performing a second function Function B, and the third instruction Inst2 performing a moving function FJUMP for executing a loop may be included. In addition, information @0 on a position of a target and information n representing the number of times of a loop may be included in the third instruction Inst2. In addition, according to the above-described embodiments, when the current program counting value is 1, together with the second instruction Inst1, the third instruction Inst2 is read and a predecoding operation may be performed.

[00124] On the other hand, in FIG. 15B, a case in which instructions including a loop instruction in a common case are processed and a case in which instructions including a loop instruction according to an exemplary embodiment of the inventive concept are processed are illustrated.

[00125] Referring to FIG. 15B, when the basic block of FIG. 15A is executed by a common method, one instruction is read from each operation timing and accordingly, the first function Function A, the second function Function B, and the moving function JUMP may be sequentially performed. On the other hand, according to an exemplary embodiment of the inventive concept, when the current program counting value instructs the second instruction Inst1, a predecoding operation on the third instruction Inst2 is performed. Accordingly, without additionally executing the moving function JUMP, the first function Function A and the second function Function B may be repeatedly performed the determined

WHAT IS CLAIMED IS:

1. A memory device comprising:

a memory comprising a memory bank including memory cells;

a processor in memory (PIM) circuit configured to process an operation using data provided by a host or data read from the memory bank, the PIM circuit including instruction memory storing at least one instruction provided from the host; and

control logic configured to decode an address, or a command and an address, received from the host to generate a decoding result and to perform a control operation so that one of i) a memory operation on the memory bank is performed and ii) the PIM circuit performs a processing operation, based on the decoding result,

wherein a counting value of a program counter instructing a position of the instruction memory is controlled in response to the address, or the command and the address, instructing the processing operation be performed.

2. The memory device of claim 1, wherein the memory device performs the memory operation when a bit value of the address belongs to a first range and performs the processing operation when the bit value of the address belongs to a second range different from the first range.

3. The memory device of claim 2, wherein the address comprises mode information representing a memory operation mode or an operation processing mode and address information representing a position of the memory bank, and

wherein the address belongs to the first range or the second range in accordance with a bit value of the mode information.

4. The memory device of any one of claims 1 to 3, wherein the command is a read command or a write command.

5. The memory device of claim 4,

wherein the PIM circuit performs the processing operation by using the data read from a position corresponding to the address of the memory bank when the command corresponds to the read command, and

wherein the PIM circuit performs the processing operation using the data provided by the host when the command corresponds to the write command.

6. The memory device of any one of claims 1 to 5, wherein the address comprises a row address instructing a row of the memory bank and a column address instructing a column of the memory bank and the PIM circuit performs the processing operation using the data read from a position instructed by the row address and the column address.

7. The memory device of any one of claims 1 to 6, wherein the PIM circuit further comprises:

a processing controller configured to perform a control operation so that an instruction operation corresponding to an instruction instructed by the counting value of the program counter is processed; and

at least one processing element configured to perform the instruction operation based on control of the processing controller.

8. The memory device of claim 7, wherein the at least one processing element comprises a plurality of processing elements, the memory comprises a plurality of memory banks including the memory bank, and the processing elements are respectively arranged to correspond to the memory banks.

9. The memory device of claim 8, wherein each of the processing elements is shared by at least two of the memory banks.

10. The memory device of any one of claims 1 to 9, wherein, when the address, or the command and the address, instructing the processing operation to be performed is received,

a first instruction instructed by a current counting value of the program counter and a second instruction instructed by a next counting value of the program counter are read together, and

a predecoding operation is performed on the second instruction.

11. The memory device of claim 10, wherein, when the second instruction

corresponds to a loop instruction, the second instruction includes information on a position of a third instruction to be moved, and

wherein the PIM circuit executes the third instruction without executing the second instruction when the address, or the command and the address, instructing a next operation to be processed is received.

12. The memory device of any one of claims 1 to 11, wherein the operation is for neural network processing, and the PIM circuit performs the processing operation using the data from the host and weight information in the memory bank.

13. A method of operating a memory device including a plurality of memory banks, the method comprising:

storing a plurality of instructions received from a host that correspond to a processing operation;

decoding an address, or a command and an address, received from the host to determine whether the address belongs to one of a first range and a second range;

performing a memory operation corresponding to the received address, or the received command and the address, when it is determined that the address corresponds to the first range; and

reading an instructed instruction among the plurality of instructions and performing a processing operation corresponding to the read instruction in a processor in memory (PIM) circuit provided in the memory device, when it is determined that the address belongs to the second range,

wherein the reading of the instruction comprises:

checking a counting value of a program counter instructing a position of instruction memory in which the plurality of instructions are stored, and

performing counting of the program counter in response to the address, or the command and the address, instructing the processing operation to be performed.

14. The method of claim 13, wherein, at least some bits of the address comprise address information on a position of data stored in a memory bank of the memory banks, and

wherein the processing operation is performed by using data read from a position instructed by the address information.

15. A data processing system comprising a host, wherein the host comprises:

address map memory configured to store a plurality of addresses that belong to a first range for instructing a memory operation to be performed on a memory device and a plurality of addresses that belong to a second range for instructing a processing operation to be performed using data read from a selected memory bank among memory banks of the memory device; and

a memory interface configured to instruct that the memory operation be performed by outputting an address that belongs to the first range and to instruct that the processing operation be performed by outputting an address that belongs to the second range,

wherein the data processing system further comprises the memory device including the plurality of banks, wherein the memory device comprises:

a processor in memory (PIM) circuit configured to process an operation by using at least one of data provided by the host and data read from the memory banks;

control logic configured to decode an address, or a command and an address, received from the host to generate a decoding result and to perform a control operation so that one of i) the memory operation on the memory banks is performed and ii) the PIM circuit performs the processing operation based on the decoding result,

wherein the PIM circuit comprises:

instruction memory configured to store a plurality of instructions provided by the host; and

a program counter configured to output a counting value instructing a position of the instruction memory, and

wherein, in response to the address, or the command and the address, instructing the processing operation to be performed, counting of the program counter is performed.

16. The data processing system of claim 15, wherein, in instructing the memory operation and the processing operation, the host further outputs a write command or a read command.

17. The data processing system of claim 15 or claim 16, wherein, in the address, or the command and the address, instructing the processing operation to be performed, address information on a position of data stored in the selected bank is included in the address,

and

wherein the PIM circuit performs the processing operation by using data read from a position corresponding to the address of the selected bank.