

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
3 November 2005 (03.11.2005)

PCT

(10) International Publication Number
WO 2005/104355 A1

(51) International Patent Classification⁷: **H03F 3/04**

Arlington Heights, IL 60004 (US). **VAN HORN, Mark, I.** [US/US]; 1805 Lakemont Drive, Arlington, TX 76013 (US).

(21) International Application Number:
PCT/US2005/002494

(74) Agents: **KING, Robert L.** et al.; 7700 W. Parmer Lane, MD: TX32/PL02, Austin, TX 78729 (US).

(22) International Filing Date: 26 January 2005 (26.01.2005)

(25) Filing Language: English

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(26) Publication Language: English

(30) Priority Data:
10/808,056 24 March 2004 (24.03.2004) US

(71) Applicant (for all designated States except US):
FREESCALE SEMICONDUCTOR, INC. [US/US];
6501 William Cannon Drive West, Austin, TX 78735 (US).

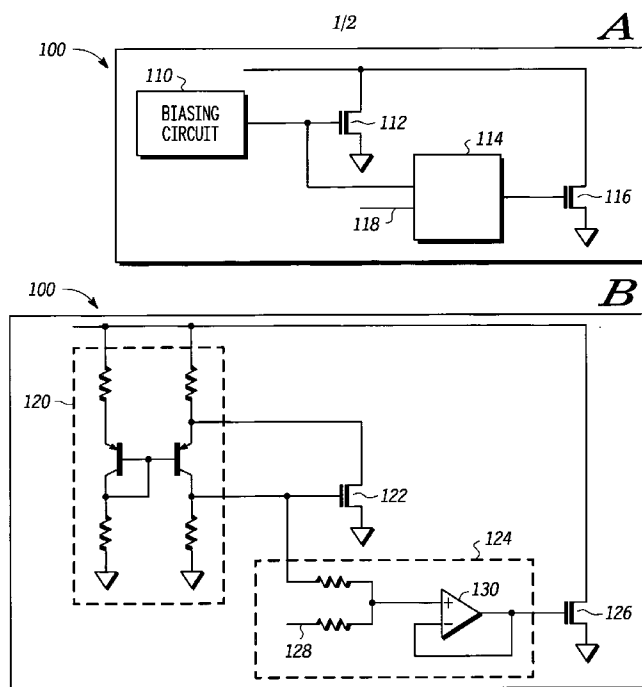
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO,

(72) Inventors; and

(75) Inventors/Applicants (for US only): **KRVAVAC, Enver** [US/US]; 1325 Marble Hill Drive, Lake Zurich, IL 60047 (US). **MITZLAFF, James, E.** [US/US]; 1727 N. Chestnut,

[Continued on next page]

(54) Title: METHOD AND APPARATUS FOR DOHERTY AMPLIFIER BIASING



(57) Abstract: Apparatus and methods are described for biasing amplifiers with multiple outputs. A semiconductor die (100) may include a reference Field Effect Transistor (FET) (112) integrated on the semiconductor die and coupled to an amplifier (116) integrated on the semiconductor die. A voltage offset circuit (114) may also be integrated on the semiconductor die (100) for determining the voltage needed to operate the amplifier (116).

WO 2005/104355 A1



SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

— *with international search report*