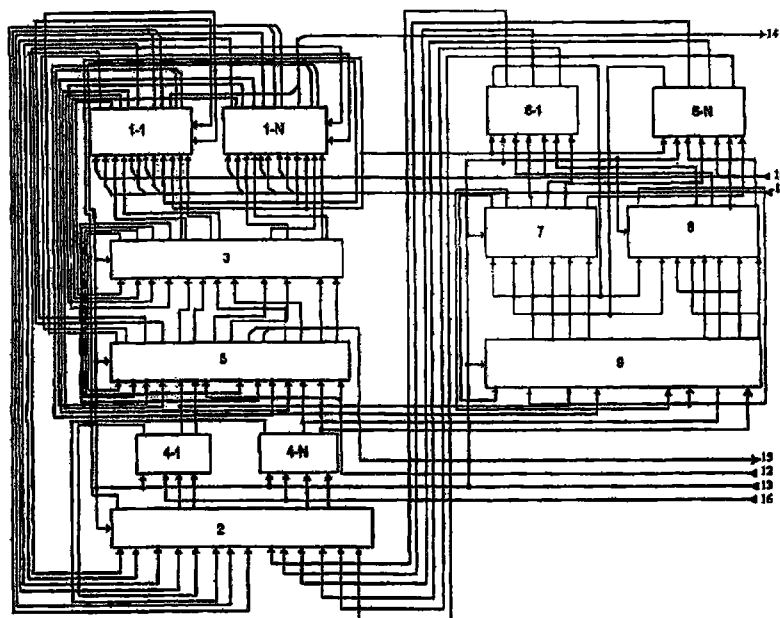




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : G06F 13/38, 13/40, 13/16, H04L 12/40, 12/56, 12/02, 12/50	A1	(11) International Publication Number: WO 99/42927 (43) International Publication Date: 26 August 1999 (26.08.99)
(21) International Application Number: PCT/US99/03633 (22) International Filing Date: 19 February 1999 (19.02.99) (30) Priority Data: 98102944 20 February 1998 (20.02.98) RU (71)(72) Applicant and Inventor: EMERALD, Robert, L. [US/US]; 25151 Iroquois Court, Barrington, IL 60010 (US). (74) Agent: COSTA, John, G.; P.O. Box 948, Highland, NY 12528 (US).		(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published With international search report.

(54) Title: COMPUTER WITH IMPROVED ASSOCIATIVE MEMORY AND SWITCH



(57) Abstract

A computer system comprising n processor units (1- n) where n is a positive integer, first switch (2), second switch (3), buffering block (5) and m associative memory modules (4- n) where m is a positive integer and using data flow control over computations and to further inclusion of processing means utilizing the von Neumann principle of computation resulting in an improvement of performance and a decrease in the volume of associative memory.