DOUBLE AND TRIPLE GATE MOSFET DEVICES AND METHODS FOR MAKING SAME

TECHNICAL FIELD

The present invention relates generally to semiconductor manufacturing and, more particularly, to double and triple gate metal-oxide semiconductor field-effect transistor (MOSFET) devices and methods of making these devices.

BACKGROUND ART

Scaling of device dimensions has been a primary factor driving improvements in integrated circuit performance and reduction in integrated circuit cost. Due to limitations associated with gate-oxide thicknesses and source/drain (S/D) junction depths, scaling of existing bulk MOSFET devices beyond the 0.1 μm process generation may be difficult, if not impossible. New device structures and new materials, thus, are likely to be needed to improve FET performance.

Double-gate MOSFETs represent new devices that are candidates for succeeding existing planar MOSFETs. In double-gate MOSFETs, the use of two gates to control the channel significantly suppresses short-channel effects. A FinFET is a recent double-gate structure that includes a channel formed in a vertical fin controlled by a self-aligned double gate. The fin may be made thin enough such that the two gates can together control the entire fully depleted channel. Although a double-gate structure, the FinFET is similar to existing planar MOSFET in layout and fabrication techniques. The FinFET also provides a range of channel lengths, CMOS compatibility, and large packing density compared to other double-gate structures.

DISCLOSURE OF THE INVENTION

Implementations consistent with the principles of the invention provide double gate and triple gate FinFET devices. Unlike conventional designs, each of the gates in the FinFET can independently control the FinFET's channel.

In accordance with the purpose of this invention as embodied and broadly described herein, a method for forming gates in a MOSFET includes forming a fin structure, forming a first gate structure on top of the fin structure, and forming a second gate structure that surrounds the fin structure and the first gate structure.

In another implementation consistent with the present invention, a method for forming gates in a MOSFET includes forming a fin, forming a first gate on top of the fin, forming a second gate that surrounds the fin and the first gate, and removing a portion of the second gate to expose the first gate, the removing causing the second gate to be split into separate gate structures.

In yet another implementation consistent with the principles of the invention, a double gate MOSFET is provided. The double gate MOSFET includes a fin, a first gate structure and a second gate structure. The first gate structure is formed on top of the fin. The second gate structure surrounds the fin and the first gate structure.

In a further implementation consistent with the principles of the invention, a triple gate MOSFET is provided. The triple gate MOSFET includes a fin, a first gate structure formed on top of the fin, a second gate structure formed adjacent the fin, and a third gate structure formed adjacent the fin and opposite the second gate structure.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate an embodiment of the invention and, together with the description, explain the invention. In the drawings,

Fig. 1 illustrates an exemplary process for fabricating a double gate MOSFET in an implementation consistent with the principles of the invention;

Figs. 2-4 illustrate exemplary cross-sectional views of a double gate MOSFET fabricated according to the processing described in Fig. 1;

Fig. 5 illustrates an exemplary process for fabricating a triple gate MOSFET in an implementation consistent with the principles of the invention;

Figs. 6-8 illustrate exemplary cross-sectional views of a triple gate MOSFET fabricated according to the processing described in Fig. 5;

Fig. 9 illustrates an exemplary structure for adding mobility to a fin in an implementation consistent with the principles of the invention; and

Figs. 10-12 illustrate exemplary cross-sectional views of a MOSFET fabricated to include a thin fin body structure.

BEST MODE FOR CARRYING OUT THE INVENTION

The following detailed description of implementations consistent with the present invention refers to the accompanying drawings. The same reference numbers in different drawings may identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and their equivalents.

Implementations consistent with the principles of the invention provide double gate and triple gate FinFET devices. Unlike conventional designs, each of the gates in the FinFET can independently control the fin channel.

EXEMPLARY PROCESSING

Fig. 1 illustrates an exemplary process for fabricating a double gate MOSFET in an implementation consistent with the principles of the invention. Figs. 2-4 illustrate exemplary cross-sectional views of a MOSFET fabricated according to the processing described in Fig. 1.

With reference to Figs. 1 and 2, processing may begin with a silicon on insulator (SOI) structure that includes a silicon substrate 200, a buried oxide layer 210 and a silicon layer 220 on the buried oxide layer 210. Buried oxide layer 210 and silicon layer 220 may be formed on substrate 200 in a conventional manner. The thickness of the buried oxide layer may range, for example, from about 100 Å to 2000 Å. Silicon layer 220 thickness may range from about 200 Å to 1000 Å. It will be appreciated that silicon layer 220 is used to form the fin.

A gate oxide layer 230 may be deposited or thermally grown on silicon layer 220 (act 105). Gate oxide layer 230 may be formed at a thickness ranging from approximately 5 Å to 50 Å. Alternatively, other gate dielectric materials, such as high-K dielectric materials, may be used. In one implementation, nitrided oxide may be used as the gate dielectric material. A gate electrode layer 240 may be deposited over gate

oxide layer 230 for forming the first gate (act 110). A number of materials may be used for gate electrode 240. For example, gate electrode 240 may be made from a metal (e.g., tungsten, tantalum, aluminum, nickel, ruthenium, rhodium, palladium, platinum, titanium, molybdenum, etc.), a metal containing a compound (e.g., titanium nitride, tantalum nitride, ruthenium oxide, etc.), or a doped semiconductor (e.g., polycrystalline silicon, polycrystalline silicon-germanium, etc.). A cover layer 250 (or hard mask) may optionally be formed on top of gate electrode 240 to aid in pattern optimization or chemical-mechanical polishing (CMP) (act 115). Cover layer 250 may, for example, include a silicon nitride (SiN) material or some other similar type of material capable of protecting the gate electrode during the fabrication process. Cover layer 250 may be deposited, for example, by chemical vapor deposition (CVD) at a thickness ranging from approximately 30 Å to 200 Å.

Fin 220 and first gate 230/240 may be patterned by conventional lithographic techniques (e.g., electron beam (EB) lithography) (act 120). Fin 220 and first gate 230 may then be etched using well-known etching techniques (act 120). The resulting structure 300 is illustrated in Fig. 3. The width of fin 220 and first gate 230 in structure 300 may be approximately 50 Å to 500 Å.

Following the formation of fin 220 and first gate 230, a second gate may be formed. A second gate oxide layer 410 may be deposited or thermally grown (act 125), as illustrated in Fig. 4. Gate oxide layer 410 may be deposited or grown to a thickness of approximately 5 Å to 50 Å. Alternatively, other gate dielectric materials may be used. For example, any high-K dielectric material may be used as the gate dielectric material. A second gate electrode layer 420 may be deposited over gate oxide layer 410 for forming the second gate (act 130). Similar to first gate electrode 240, a number of materials may be used for second gate electrode 420. As a result, this structure 400 allows two gates (i.e., gates 240 and 420) to independently control the fin channel. Conventional MOSFET fabrication processing can be utilized to complete the transistor (e.g., forming the source and drain regions), contacts, interconnects and inter-level dielectrics for the double gate MOSFET.

Fig. 5 illustrates an exemplary process for fabricating a triple gate MOSFET in an implementation consistent with the principles of the invention. Figs. 6-8 illustrate exemplary cross-sectional views of a triple gate MOSFET fabricated according to the processing described in Fig. 5. Processing may begin by performing acts 105-130 described above with respect to Fig. 1. After gate electrode layer 420 has been deposited, an interlayer dielectric (ILD) 610 may be deposited over second gate electrode layer 410 (act 505), as illustrated in Fig. 6. ILD 610 may include, for example, tetraethoxy silane (TEOS) or another similar type of material. The thickness of ILD 610 may be such that it extends above the height of second gate electrode 420.

Chemical-mechanical polishing (CMP) or another comparable technique may then be performed to planarize the wafer surface to expose first gate electrode 240 (act 510), as illustrated in Fig. 7. As a result, second gate electrode 420 may be split to form two separate gate structures, namely gates 720 and 730. Based on this configuration, a triple gate MOSFET may be formed, where the first gate electrode 240 acts as a third gate 710. Gates 710-730 may each independently control fin 220. To reduce capacitive coupling to gate 710, gates 720 and 730 may be etched back (act 515), as illustrated in Fig. 8, using known techniques.

Conventional MOSFET fabrication processing can be utilized to complete the transistor (e.g., forming the source and drain regions), contacts, interconnects and inter-level dielectrics for the triple gate MOSFET.

OTHER IMPLEMENTATIONS

Mobility is an important attribute for improving transistor performance. Mobility may be affected by the state of the strain (or stress) in the film. For example, tensile strain is good for electron mobility, while compressive stress may aid hole mobility.

Fig. 9 illustrates an exemplary structure for adding mobility to a fin. As illustrated, a fin structure 910 may be formed by forming a silicon layer on a semiconductor substrate. In one implementation consistent with the invention, the semiconductor substrate may be a SOI structure including an insulating layer, such as a buried oxide layer, formed at a thickness ranging from 100 Å to 2000 Å. Processing for forming a semiconductor substrate, having a buried oxide layer, is well known in the integrated circuit fabrication arts.

A highly stressed film (referred to hereinafter as a "capping layer") 920 may then be formed on top of fin structure 910. In one implementation, capping layer 920 may be formed from, for example, a nitride-based material at a thickness of approximately 100 Å to 1000 Å. Other materials may alternatively be used. Capping layer 920 remains after fin 910 is etched so that fin 910 is strained to improve mobility.

Figs. 10-12 illustrate exemplary cross-sectional views of a MOSFET fabricated to include a thin fin body structure. As illustrated in Fig. 10, a source region 1010, a drain region 1020, and a fin structure 1030 may be formed via conventional fabrication techniques. For example, an SOI structure may include an insulating layer (e.g., a buried oxide layer) formed on a semiconductor substrate. A silicon film may be formed on the SOI structure. A hard mask (e.g., silicon dioxide) may be deposited on the silicon film. Fin structure 1030 may then be formed via, for example, e-beam lithography and etching. Source and drain regions 1010 and 1020 may then be formed in a similar manner.

Once source region 1010, drain region 1020, and fin structure 1030 have been formed, source region 1010 and drain region 1020 may be covered with a protective mask, as illustrated in Fig. 11. A number of materials may be used for the protective mask, such as a silicon nitride based material. The thickness of the unprotected fin structure 1030 may then be reduced to form a thin fin structure 1230, as illustrated in Fig. 12. This thinning of fin structure 1030 may be accomplished via etching or some other well known technique.

CONCLUSION

Implementations consistent with the principles of the invention provide double gate and triple gate FinFET devices. Unlike conventional designs, each of the gates in the FinFET can independently control the fin channel.

The foregoing description of exemplary embodiments of the present invention provides illustration and description, but is not intended to be exhaustive or to limit the invention to the precise form disclosed. Modifications and variations are possible in light of the above teachings or may be acquired from practice of the invention. For example, in the above descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the

present invention. However, the present invention can be practiced without resorting to the details specifically set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention. In practicing the present invention, conventional deposition, photolithographic and etching techniques may be employed, and hence, the details of such techniques have not been set forth herein in detail.

While series of acts have been described with regard to Figs. 1 and 5, the order of the acts may be varied in other implementations consistent with the present invention. Moreover, non-dependent acts may be implemented in parallel.

No element, act, or instruction used in the description of the present application should be construed as critical or essential to the invention unless explicitly described as such. Also, as used herein, the article "a" is intended to include one or more items. Where only one item is intended, the term "one" or similar language is used.

The scope of the invention is defined by the claims and their equivalents.

CLAIMS:

1. A method for forming gates in a metal-oxide semiconductor field-effect transistor (MOSFET), the method characterized by:

forming a silicon fin structure by forming a silicon layer on an insulating layer that is formed over a semiconductor substrate;

forming a first gate structure on top of the fin structure, a width of the first gate structure being substantially similar to a width of the fin structure; and

forming a second gate structure that surrounds the fin structure and the first gate structure.

2. The method of claim 1, wherein the forming a first gate structure includes:

forming a dielectric layer on the silicon layer,

depositing a gate electrode layer over the dielectric layer, and

patterning the gate electrode layer.

3. The method of claim 1, wherein the forming a second gate structure includes:

forming a second dielectric layer to surround the fin structure and the first gate structure,

depositing a second gate electrode layer over the second dielectric layer, and

patterning the second gate electrode layer.

4. The method of claim 1, wherein the first gate structure and the second gate structure are positioned adjacent the fin.

5. The method of claim 1, further comprising:

independently controlling the fin with the first gate structure and the second gate structure.

6. A method for forming gates in a metal-oxide semiconductor field-effect transistor (MOSFET), the method characterized by:

forming a fin;

forming a first gate on top of the fin;

forming a second gate that surrounds the fin and the first gate; and

removing a portion of the second gate to expose the first gate, the removing causing the second gate to be split into separate gate structures.

7. The method of claim 6, wherein the forming a fin includes:

forming a silicon layer on an insulating layer that is formed over a semiconductor substrate.

8. The method of claim 7, wherein the forming a first gate includes:

forming a dielectric material on the silicon layer, and

depositing a gate electrode layer over the dielectric material.

9. The method of claim 6, wherein the forming a second gate includes:

forming a second dielectric material to surround the fin and the first gate, and

depositing a second gate electrode layer over the second dielectric material.