DYNAMIC SYNCHRONIZATION OF DATA CAPTURE ON AN OPTICAL OR OTHER HIGH SPEED COMMUNICATIONS LINK

TECHNICAL FIELD

The present invention relates generally to data communications systems, and more specifically to synchronizing a data communications system to ensure data signals transferred by the system are successfully transferred.

BACKGROUND OF THE INVENTION

A conventional computer system 100 includes a processor 102 coupled through a system bus 104 to a system memory 106 as illustrated in Figure 1. The system memory 106 includes a memory controller 108 coupled to the system bus 104 and coupled to three memory modules 110A-C though a common data bus DQ, address bus ADDR, and control bus CONT. Each memory module 110A-C includes a plurality of individual memory devices 112, one of which is shown on the memory module 110A. Each of the memory devices 112 is typically a dynamic random access memory (DRAM) since DRAMs form the largest portion of system memory 106 because they provide large storage capacity at relatively inexpensive prices. In response to a request from the processor 102, the memory controller 108 initiates a memory operation by providing a memory command in the form of control signals and a memory address (generally in the form of a row address and a column address) on the control bus CONT and address bus ADDR, respectively, to all of the memory modules 110A-C. If the memory operation is a write operation, the memory controller 108 will also apply write data to the memory modules 110A-C through the data bus DQ. To prevent all of the memory modules 110A-C from responding to the memory command, the memory controller 108 also generally applies a unique chip select or similar select signal over the control bus CONT to each of the memory modules 110A-C so that only the memory module receiving an active chip select signal responds to the

memory command. Each memory module 110A-C may receive more than one chip select signal, with each group of memory devices 112 receiving the same chip select signal being designated a "rank" of memory.

Conventional processors 102 generally operate at a relatively high speed compared to the memory modules 110A-C. Because access to system memory 106 is a frequent operation of the processor 102, the slower operating speed of the memory 110A-C greatly slows the overall operation of the computer system 100, as will be appreciated by those skilled in the art. As a result, much effort has been put into increasing the data transfer rate or bandwidth of the data bus DQ to enable system memory 106 to transfer data more quickly. To increase the bandwidth of the data bus DQ, the width of the data bus has been increased, and new types of DRAM technology having much higher transfer speeds, such as RAMBUS DRAMs ("RDRAMs") and synchronous link DRAMs ("SLDRAMs"), have also been developed. As the operating speed of the data bus DQ increases, however, noise, signal skew, a smaller data eye--which defines the duration for which the data signals are valid--and other factors make it more difficult to reliably transfer data over the data bus.

One approach that has been utilized in transferring data more reliably at high data transfer rates is an adaptive process of adjusting the delay between data signals and a clock signal transmitted along with the data signals. A receiving device captures the data signals in response to the clock signal. The process involves applying the clock signal and a pseudorandom bit pattern having known values on the data bus DQ. The timing relationship or delay between the data signals forming the pseudorandom bit pattern and the clock signal is thereafter adjusted through a series of values, and the bit pattern captured at each value of the delay. Because the pseudorandom bit pattern has known values, the captured data can be compared to the expected values to determine whether the bit pattern was successfully captured at each value of the delay between the bit pattern and the clock signal. The values for the delay between the bit pattern and the clock signal where the bit pattern was unsuccessfully captured are designated failing values, and the values where the bit pattern was successfully captured are designated passing values. The range of the

passing values define the data eye of the applied bit pattern, and a final value of the delay between the bit pattern and the clock signal may be selected in the middle of the data eye to optimize the delay for successful capture of the bit pattern. This approach is described in more detail in U.S. Patent No. 6,338,127 to Manning entitled METHOD AND APPARATUS FOR RESYNCHRONIZING A PLURALITY OF CLOCK SIGNALS USED TO LATCH RESPECTIVE DIGITAL SIGNALS, AND MEMORY DEVICE USING SAME, and in U.S. Patent No. 6,374,360 to Keeth *et al.* entitled METHOD AND APPARATUS FOR BIT-TO-BIT TIMING CORRECTION OF A HIGH SPEED MEMORY BUS, both of which are incorporated herein by reference.

In addition to systems communicating via electrical signals, such as the RDRAM and SLDRAM technologies mentioned above, optically-based memory systems including an optical communications link between the memory controller 108 and memory modules 110A-C have also been developed to increase the bandwidth of system memory 106. In such optically-based systems, however, problems of transmitting and receiving optical signals between the memory controller 108 and the memory modules 110A-C result in unacceptably high bit error rates (BER) and continue to hamper the commercialization of such systems, particularly in system memories 106 having parallel, closely-spaced memory modules of the type found in many existing personal computer systems. For example, in an optically-based system the optical transmitter and receiver must be designed to have sufficient dynamic range to accommodate all possible variations in system memory parameters such as the total number of memory modules. Dynamic range defines the required operating range of a parameter of the receiver or transmitter, such as required power of a received optical signal for a receiver, as will be understood by those skilled in the art. Sufficient dynamic range is required to ensure optical signals are reliably transmitted and received, and transmitters and receivers having larger dynamic range are more costly, increasing the overall cost of optically-based memory systems.

There is a need for a system memory that reliably transfers data at a high bandwidth but has a relatively low cost for use in computer systems and other cost-sensitive applications.

SUMMARY OF THE INVENTION

According to one aspect of the present invention, a method dynamically adjusts link control parameters of a communications network. The communications network includes a transmitter coupled through a first data link to a receiver, with the transmitter and receiver each have at least one associated link control parameter that affects the operation of that component. Data signals are transmitted over the first data link and the transmitted data signals are captured. The values of the captured data signals are compared to expected values for those signals, and the values of the link control parameters are adjusted to successfully capture the transmitted digital signals.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a functional block diagram of a portion of a conventional computer system including a system memory having a memory controller coupled through address, control, and data busses to a number of memory modules.

Figure 2 is a functional block diagram of a portion of a system memory that executes an adaptive synchronization process of an optical communications link according to one embodiment of the present invention.

Figure 3 is a flow chart illustrating the synchronization process executed by the system memory of Figure 2 according to one embodiment of the present invention.

Figure 4 is a functional block diagram of a computer system including the system memory of Figure 2.

DETAILED DESCRIPTION OF THE INVENTION

Figure 2 is a functional block diagram of a portion of a system memory 200 including an optical communications link 202 for transferring data between a memory controller 204 and a memory device 206 according to one embodiment of the present invention. The optical communications link 202 includes an optical transmitter 208 that transfers write data from the memory controller 204 through a fiber-optic cable 210 or other suitable optical transmission medium to an optical receiver 212 which, in turn, provides the write data to the memory device 206, as will be described in more detail below. The optical communications link 202 further includes an optical transmitter 214 for transferring read data from the memory device 206 through the fiber-optic cable 210 to an optical receiver 216, which then provides the read data to the memory controller 204. Unlike prior optically-based memory systems, the system memory 200 executes an adaptive synchronization process of adjusting various operating parameters of the optical transmitters 208, 214 and optical receivers 212, 216 to reduce the bit error rate, lower the power consumption, and provide dynamic compensation for temperature and aging affects in the optical communications link, as will be described in more detail below. The system memory 200 executes this adaptive process to optimize the performance of the optical communications link 202 which, in turn, improves overall performance of the system memory by providing reliable high bandwidth data transfer between the memory controller 204 and memory device 206. During the adaptive process executed by the system memory 200, the memory device 206 provides to the memory controller 204 an error signal ES indicating whether particular data signals were successfully transferred over the optical communications link, as will be discussed in more detail below.

In the system memory 200, the optical communications link 202 corresponds to a data bus DQ for transferring data between the memory controller 204 and memory device 206. An address bus ADDR and control bus CONT are electrical busses through which the memory controller 204 applies address and control signals, respectively, to the memory device 206. With other embodiments of the system memory 200, the

communications link 202 also includes the address and control busses ADDR, CONT for communicating address and control signals from the memory controller 204 to the memory device 206. Although only the single memory device 206 is depicted in Figure 2, this is done merely for ease of illustration and description of the system memory 200, and the system memory would normally include one or more memory modules (see Figure 1) each containing a plurality of memory devices. The memory controller 204 generates a plurality of control signals 218 that are applied to the transmitters 208, 214 and receivers 212, 216 to adjust the link control parameters of these components. In the following description of several embodiments of the present invention, certain details are set forth to provide a sufficient understanding of the invention, but one skilled in the art will appreciate that the invention may be practiced without these particular details. In other instances, the operation of well known components has not been shown or described in detail to avoid unnecessarily obscuring the present invention.

Before describing the overall adaptive synchronization process executed by the system memory 200, the operation of the optical transmitters 208, 214 and optical receivers 212, 216 will be described in more detail. Operation of the optical transmitters 208 and 214 is the same, as is the operation of the optical receivers 212 and 216, and thus, for the sake of brevity, only the operation of the transmitter 208 and receiver 212 will be described in more detail. The optical transmitter 208 receives a bit stream of electrical data signals from the memory controller 204, modulates an optical carrier signal with the received bit stream, and couples the modulated optical carrier into the fiber-optic cable 210. Typically, the optical transmitter 208 includes a light emitting diode (LED) or laser diode for generating the optical carrier signal. The optical transmitter 208 includes several operational parameters whose values are typically defined during design of the system containing the optical transmitter.

One such operational parameter of the optical transmitter 208 is a gain of the transmitter and determines the power of a light corresponding to the optical carrier signal that is coupled into the fiber-optic optic cable 210. The transmitter 208 must provide an

optical carrier signal having sufficient power to propagate through the fiber-optic cable 210 and be received by the optical receiver 212. The gain of the optical transmitter 208 ensures the optical carrier signal a sufficient power to compensate for various losses in the communications link 202, such as attenuation in the fiber-optic optic cable 210 and losses resulting from inefficient coupling of the optical transmitter to the fiber-optic cable. Another operational parameter of the optical transmitter 208 is a pulse-shaping parameter that ensures the optical transmitter 208 generates an optical carrier signal having the required shape to allow the carrier signal to be reliably detected and demodulated by the optical receiver 212. When an LED is used as the light generation source in the optical transmitter 208, the pulse-shaping parameter compensates for differing turn ON and OFF times of the LED.

The optical receiver 212 senses or detects the received modulated optical carrier signal propagating through the fiber-optic optic cable 210, converts the modulated optical carrier signal into corresponding electrical signals, and demodulates the signal to obtain the originally transmitted data signals. Typically, the optical receiver 212 includes a photo diode for detecting the received modulated optical carrier signal. One operational parameter associated with the optical receiver 212 is an input threshold level or sensitivity that defines a minimum optical power the receiver can reliably detect at a given data rate in order to achieve a particular bit error rate. The optical receiver 212 may also include a link monitor, which is circuitry indicating when the received modulated optical carrier signal from the fiber-optic cable 210 is less than the required minimum optical power. Suitable circuitry for forming all components 202-216 in the system memory 200 will be understood by those skilled in the art, and thus, for the sake of brevity, such circuitry will not be described or depicted in more detail.

The overall process executed by the system memory 200 in adaptively adjusting the operational parameters of the optical transmitters 208, 214 and optical receivers 212, 216 will now be described in more detail with reference to the flowchart of Figure 3. In the following description, the operational parameters of the transmitters 208,

214 and receivers 212, 216, may alternately be referred to as link control parameters since the values of these parameters affect or control the overall operation of the optical communications link 202. The process executed by the system memory 200 during write operations in synchronizing the transfer of write data from the memory controller 204 through the optical transmitter 208, cable 210, and optical receiver 212 to the memory device 206 will now be described in more detail with reference to Figure 3. The process begins in step 300 and proceeds immediately to step 302 in which the memory controller 204 (Figure 2) initializes the values of the various link control parameters associated with the optical transmitter 208 and optical receiver 212. Once the link control parameters have been initialized, the process goes to step 304 and the memory controller 204 applies synchronization data to the optical transmitter 208 in the form of a pseudorandom bit pattern. Such synchronization data may, for example, be a pseudorandom bit pattern including a known repeating sequence of pseudorandom bits. One suitable pseudorandom bit pattern is the pattern utilized in synchronizing SLDRAM memory devices, as will be understood by those skilled in the art. In response to the applied synchronization data, the optical transmitter 208 modulates the optical carrier signal which, in turn, is propagated through the fiber-optic cable 210 to the optical receiver 212.

From step 304, the process goes to step 306 and the memory device 206 captures the synchronization data transmitted over the optical communications link 202. More specifically, the optical receiver 212 detects, converts, and demodulates the received modulated optical carrier signal to obtain electrical received data signals that ideally should correspond to the originally transmitted synchronization data. The process proceeds to step 308 in which the electrical received data signals from the optical receiver 212 are transferred to the memory device 206 which, in turn, compares the values of the received data signals to expected values for those signals. The synchronization data has known values, and thus the memory device 206 is able to generate the expected values for the received data signals. For example, when the synchronization data is a pseudorandom bit

pattern having a known repeating sequence of bits, the memory device 206 can determine expected values for the received data signals.

When the determination in step 308 is negative, meaning the received data signals do not equal the expected values for those signals, the process goes to step 310 and the memory device 206 activates the error signal ES. If the determination in step 308 is positive, which means the received data signals are equal to the expected values for those signals, the process goes to step 312 and the memory device 206 deactivates the error signal ES. From either step 310 or step 312, the process of proceeds to step 314 and the current value of the error signal ES associated with the current values of a link control parameters is stored. Note, the values of the error signal ES can be stored in the memory device 206 and later transferred to the memory controller 204 to these values may be transferred as they are generated. In the embodiment of Figure 2, the error signal ES is an electrical signal and is applied to the memory controller 204 through a conventional electrical bus and not through the optical communications link 202.

After the value of error signal ES associated with the current link control parameters has been stored in step 314, the process goes to step 316 and the memory controller 204 and determines whether all values of the link control parameters have been tested. This determination indicates whether each link control parameter has been assigned every possible value within a possible range of values for the parameter. When the determination in step 316 is negative, the process goes to step 318 and the memory controller 204 adjusts the values of one or more link control parameters. The process then goes back and repeats steps 304-316 for the new values of the link control parameters established in step 318. In this way, the memory controller 204 repeatedly adjusts the values of link control parameters and thereafter transmits synchronization data to the memory device 206 through the optical communications link 202 which now operates according to the new values for the link control parameters. Each time the values of link control parameters are adjusted, the memory device 206 determines whether the received electrical data signals have their expected values and stores the error signal ES having the

appropriate value that is associated with the current link control parameters. An array of error signals ES is thus generated, with the value of each error signal in the array being associated with particular values for the link control parameters.

The process continues executing steps 304-316 until the determination in step 316 is positive, meaning that all link control parameters have assumed all desired values. Thus, when the optical communications link 202 has been tested for all desired values of the link control parameters, the determination in step 316 is positive and the process proceeds to step 319. In step 319, if the memory controller 204 does not already contain the array of error signals ES generated during steps 304-316, the error signals are transferred to the memory controller 204. At this point, the memory controller 204 evaluates the array of error signals ES to determine optimal values for the link control parameters. The process then proceeds to step 320 and the memory controller 204 sets each of the link control parameters for the optical transmitter 208 and optical receiver 212 to the determined optimal value. From step 320, the synchronization process goes to step 322 and terminates, with the link control parameters of the optical transmitter 208 and optical receiver 212 having been set to values to be utilized during normal operation of the system memory 200.

Once the link control parameters of the optical transmitter 208 and optical receiver 212 have been set, the system memory 200 executes substantially the same process just described to adjust the link control parameters of the optical transmitter 214 and optical receiver 216 to optimal values and thereby synchronize the optical communication link 202 for read data transfer operations. Because the process of setting the link control parameters of the optical transmitter 214 and optical receiver 216 is substantially the same as just described and will be understood by those skilled in the art, this process will not, for the sake of brevity, be described in more detail.

The times at which the system memory 200 (Figure 2) executes the synchronization process may be varied, and may be done, for example, upon initial power up of the system memory, periodically, or may be done in response to some other factor

(*e.g.*, voltage drifting outside a particular range). Moreover, the specific synchronization process, including which link control parameters are adjusted and the order in which such parameters are adjusted, may vary, as will be appreciated by those skilled in the art. In one embodiment, the system memory 200 adjusts the gain and pulse-shaping parameters of the optical transmitters 208, 214 and the sensitivity of the optical receivers 212, 216 are adjusted. In this embodiment, the synchronization process may adjust each link control parameter over its entire permissible range and store the associated error signals ES for that parameter. Each link control parameter is then set to a value in the middle of a "passing" range, which corresponds to a group of inactive ES signals for consecutive increments of the associated parameter. An iterative process could then be utilized to optimize all the link control parameters starting from these initial values. Alternatively, a prioritization algorithm can be executed by the system memory 200 in adjusting the link control parameters. For example, all link control parameters could be set to initial nominal values, the sensitivity of the optical receivers 212, 216 adjusted first to achieve low power consumption by the receivers. The gain of the optical transmitters 208, 214 could be adjusted next, with the pulse-shaping parameter adjusted last to effectively obtain vernier improvements of performance given the first two parameters. Another approach would be to try every possible combination of values for the gain, pulse-shaping, and sensitivity parameters, and establish the largest range of passing values for each parameter for all possible values of the other two parameters. This approach may be slow, however, given the potentially large number of combinations to be tried.

Referring back to Figure 2, the adaptive synchronization process executed by the system memory 200 reduces the bit error rate of the optical communication link 202 by dynamically adjusting the link control parameters of the optical transmitters 208, 214 and optical receivers 212, 216 since a final value for each parameter is dynamically determined and thereafter utilized during normal operation of the system memory. The process also results in lower power consumption by the system memory 200 since the adjustment of the link control parameters optimizes the operation of the link 202 instead of

assigning link control parameters of components 208-216 within the link predetermined values that must ensure proper operation for all configurations of the system memory 200. For example, by adaptively adjusting the gain of the optical transmitters 208, 214, the power consumption of the transmitters is decreased since the transmitter need not provide a fixed amount of optical energy to ensure proper operation, unlike in conventional optical communications links where the transmitter supplies a minimum amount of optical power, which may be more power than is needed in some configurations. The dynamic synchronization process of the system memory 200 also adjusts for the affects of temperature, voltage, and aging affects of components 208-216 in the optical communications link 202, which may vary as a function of time.

The process for synchronizing the optical communications link 202 may also be combined with a synchronization process for adjusting the delay between the electronic data signals and a clock signals transmitted along with those electronic data signals. Such a synchronization process for electrical data signals and a clock signal was previously discussed with reference to the conventional system memory 106 of Figure 1. In the system memory 200 of Figure 2, the transfer of the electrical data signals between the memory controller 204 and the transmitter 208 and receiver 216 would typically be done responsive to an accompanying clock signal, as would the transfer of electrical data signals between the receiver 212 and transmitter 214 and the memory device 206. Thus, the synchronization process for the link control parameters may be combined with this other synchronization process to further improve reliability of the system memory 200. For example, the link control parameters of the transmitters 208, 214, and receivers 212, 216 may first be set according the above process. The values of the link control parameters may affect the delays introduced by the transmitters 208, 214, and receivers 212, 216. Thus, after the link control parameters are set, the transfer of data signals and clock signal can be synchronized for the transfer of data between the memory controller 204 and the transmitter 208, receiver 216 and for the transfer of electrical data signals between the receiver 212, transmitter 214 and the memory device 206.

Figure 4 is a functional block diagram of a computer system 400 including the system memory 200 of Figure 2. The computer system 400 includes computer circuitry 402 for performing various computing functions, such as executing specific software to perform specific calculations or tasks. In addition, the computer system 400 includes one or more input devices 404, such as a keyboard or a mouse, coupled to the computer circuitry 402 to allow an operator to interface with the computer system. Typically, the computer system 400 also includes one or more output devices 406 coupled to the computer circuitry 402, such output devices typically being a printer or a video terminal. One or more data storage devices 408 are also typically coupled to the computer circuitry 402 to store data or retrieve data from external storage media (not shown). Examples of typical storage devices 408 include hard and floppy disks, tape cassettes, and compact disk read only memories (CD-ROMs). The computer circuitry 402 is typically coupled to the system memory 200 through a conventional electronic control, data, and address busses to provide for writing data to and reading data from the system memory.

As previously mentioned, the optical communications link 202 could include other suitable transmission media in place of the fiber-optic cable 210 such as free space. Moreover, although the system memory 200 is described and depicted as including the optical communications link 202, other high speed communications links such as a radio frequency or microwave link could be utilized in place of the optical communications link. The concepts described above are equally applicable for adaptively adjusting the operational parameters of such a radio frequency, microwave, or other high speed communications link, as will be appreciated by those skilled in the art. Even though various embodiments and advantages of the present invention have been set forth in the foregoing description, the above disclosure is illustrative only, and one skilled in the art will understand various equivalents and modifications of the described components and concepts that may be made in detail and yet remain within the broad principles of the invention. For example, some of the components described above may be implemented using either digital or analog circuitry, or a combination of both, and also, where

appropriate, may be realized through software executing on suitable processing circuitry. Therefore, the present invention is to be limited only by the appended claims.

CLAIMS

1. A method of dynamically adjusting operating parameters of a communications link including a transmitter coupled through a data link to a receiver, each of the transmitter and receiver having at least one associated link control parameter that affects its operation, the method comprising:

setting each link control parameter to an initial value;

transmitting data signals over the data link;

receiving the data signals transmitted over the data link;

determining whether the received data signals were successfully communicated over the data link;

adjusting the values of the link control parameters;

repeating the operations of transmitting data signals over the data link to adjusting the values of the link control parameters;

determining final values of the link control parameters for the transmitter and receiver from the operations of determining whether the received data signals were successfully communicated over the data link associated with each of the adjusted values of the link control parameters; and

setting each of the link control parameters to the determined final value.

2. The method of claim 1 wherein the communications link comprises an optical communications link.

3. The method of claim 2 wherein the adjusted link control parameters include a gain and a pulse shaping parameter associated with the transmitter, and an input threshold parameter associated with the receiver.

4. The method of claim 2 wherein the optical communications link includes a fiber-optic cable.

5. The method of claim 1 wherein the data signals transmitted over the link comprise a pseudo random bit pattern having a known repeating pattern.

6. The method of claim 1 wherein determining whether the received data signals were successfully communicated over the data link comprises comparing the received data signals to expected values for the received data signals.

7. The method of claim 1 wherein adjusting the value of the link control parameters comprises adjusting the value of each parameter over an entire range of values for that parameter.

8. The method of claim 7 wherein determining whether the received data signals were successfully communicated over the data link comprises generating an error signal indicating whether the data signals were successfully captured, each error signal being associated with particular values of the link control parameters.

9. The method of claim 8 wherein determining final values of the link control parameters for the transmitter and receiver comprises selecting a final value for each link control parameter that is in the middle of a passing range of the error signals for this parameter.

10. The method of claim 1 wherein the each link control parameter is assigned a priority, and wherein the order in which final values for the link control parameters is

determined by the priorities assigned to the parameters, with link control parameters having higher assigned priorities being determined before link control parameters having lower assigned priorities.

11. The method of claim 10 wherein the link control parameters comprise a gain and a pulse-shaping parameter associated with the transmitter and an input threshold parameter associated with the receiver, and wherein the input threshold parameter is assigned a first priority, the gain is assigned a second priority, and the pulse-shaping parameter a third priority, the first priority being greater than the second priority and the second priority being greater than the third priority.

12. The method of claim 1 further comprising after each of the link control parameters is set to the determined final value, repeating the overall method after a time T to determine new values for the link control parameters.

13. The method of claim 1 further comprising after each of the link control parameters is set to the determined final value, repeating the overall method in response to a system parameter.

14. The method of claim 13 wherein the system parameter comprises a voltage and wherein the method is repeated responsive to the voltage having a value outside a defined range.

15. A system memory, comprising:

a data link;

a transmitter coupled to the data link and operable to receive data and communicate the data through the data link;

a receiver coupled to the data link to receive data from the data link and operable to output the received data;

a memory coupled to the receiver in the communications link, the memory operable during a synchronization mode to receive data from the receiver and compare the received data to expected values for the data, the memory generating an error signal responsive to the comparison; and

a memory controller coupled to the transmitter and receiver and coupled to the memory, the memory controller operable during the synchronization mode to apply a bit pattern to the transmitter and to apply control signals to adjust the values of the link control parameters of the transmitter and receiver, and the memory controller adjusting the link control parameters to final values using the values of the generated error signals from the memory.

16. The system memory of claim 15 wherein the data link comprises a fiber-optic cable and wherein the transmitter and receiver comprise an optical transmitter and optical receiver, respectively.

17. The system memory of claim 16 wherein the memory controller is configured to adjust a gain and a pulse shaping link control parameter associated with the transmitter, and an input threshold link control parameter associated with the receiver.

18. The system memory of claim 15 wherein the memory comprises a dynamic random access memory.

19. The system memory of claim 18, wherein the memory comprises a memory module including a plurality of dynamic random access memories.

20. The system memory of claim 15 wherein the data communicated over the communications link comprise data, address, and control signals.

21. The system memory of claim 15 wherein the memory controller is electrically coupled to the memory through address and control busses.

22. The system memory of claim 21 wherein the memory controller is electrically coupled to the memory to receive the error signal.

23. The system memory of claim 15 wherein the data link comprises a radio frequency communication link and wherein the transmitter and receiver comprise a radio frequency transmitter and radio frequency receiver, respectively.

24. The system memory of claim 15 wherein the bit pattern applied to the transmitter comprises a pseudo random bit pattern having a known repeating sequence.

25. The system memory of claim 15 wherein the memory controller adjusts the value of the value of each link control parameter over an entire range of values for that parameter.

26. The system memory of claim 15 wherein the memory controller adjusts the final value for each link control parameter to a value that is in the middle of a passing range of the associated error signals for this parameter.

27. The system memory of claim 15 wherein each link control parameter is assigned a priority, and wherein the order in the memory controller adjusts the final values for the link control parameters is determined by the priorities assigned to the parameters, with the link control parameters having higher assigned priorities being determined before link control parameters having lower assigned priorities.

28. The system memory of claim 27 wherein the link control parameters adjusted by the memory controller comprise a gain and a pulse-shaping parameter associated with the transmitter and an input threshold parameter associated with the receiver, and wherein the input threshold parameter is assigned a first priority, the gain is assigned a second priority,

and the pulse-shaping parameter a third priority, the first priority being greater than the second priority and the second priority being greater than the third priority.

29. The system memory of claim 15 wherein the memory controller and memory periodically operate in the synchronization mode to adjust the final values of the link control parameters.

30. The system memory of claim 15 wherein the memory controller and memory periodically operate in the synchronization mode responsive to a system parameter to adjust the final values of the link control parameters.

31. The system memory of claim 30 wherein the system parameter comprises a voltage and wherein the memory controller and memory enter the synchronization mode responsive to the voltage having a value outside a defined range.

32. The system memory of claim 15 further comprising a second transmitter coupled to the memory and coupled to the data link, and a second receiver coupled to the memory controller and the data link.

33. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a system memory coupled to the processor bus, the system memory including,

a data link;

a transmitter coupled to the data link and operable to receive data from the processor over the processor bus and communicate the data through the data link;

a receiver coupled to the data link to receive data from the data link and operable to output the received data;

a memory coupled to the receiver, the memory operable during a synchronization mode to receive data from the receiver and compare the received data to expected values for the data, the memory generating an error signal responsive to the comparison; and

a memory controller coupled to the transmitter, receiver, and the memory, the memory controller operable during the synchronization mode to apply a bit pattern to the transmitter over the processor bus and to develop control signals to adjust the values of the link control parameters of the transmitter and receiver, and the memory controller adjusting the link control parameters to final values using the values of the generated error signals from the memory.

34. The computer system of claim 33 wherein the data link comprises a fiber-optic cable and wherein the transmitter and receiver comprise an optical transmitter and optical receiver, respectively.

35. The computer system of claim 34 wherein the memory controller adjusts a gain and a pulse shaping link control parameter associated with the transmitter, and an input threshold link control parameter associated with the receiver.

36. The computer system of claim 33 wherein the memory comprises a dynamic random access memory.

37. The computer system of claim 36 wherein the memory comprises a memory module including a plurality of dynamic random access memories.

38. The computer system of claim 33 further comprising a second transmitter coupled to the memory and coupled to the data link, and a second receiver coupled to the memory controller and the data link.

39. The computer system of claim 38 wherein the error signal is coupled to the memory controller through the second transmitter, data link, and second receiver.

40. The computer system of claim 33 wherein the memory controller is electrically coupled to the memory through address and control busses.

41. The computer system of claim 40 wherein the memory controller is electrically coupled to the memory to receive the error signal.