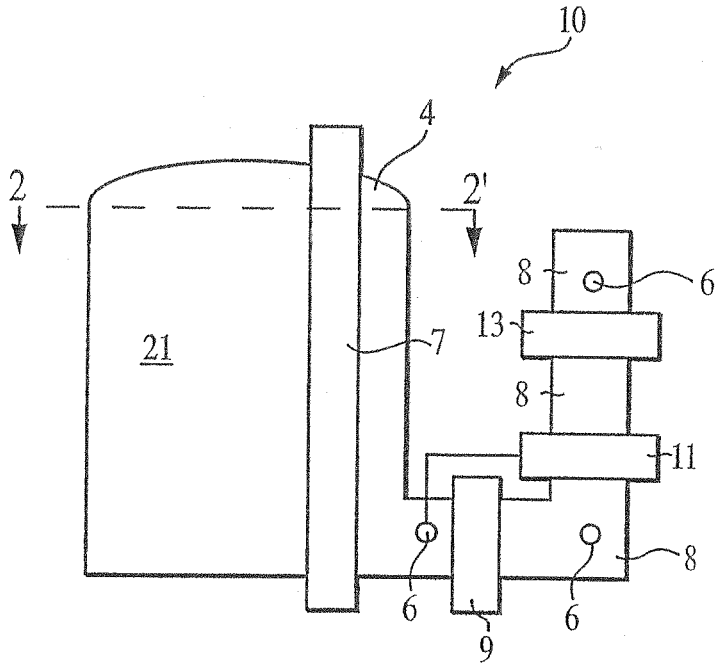


FIG. 1
PRIOR ART

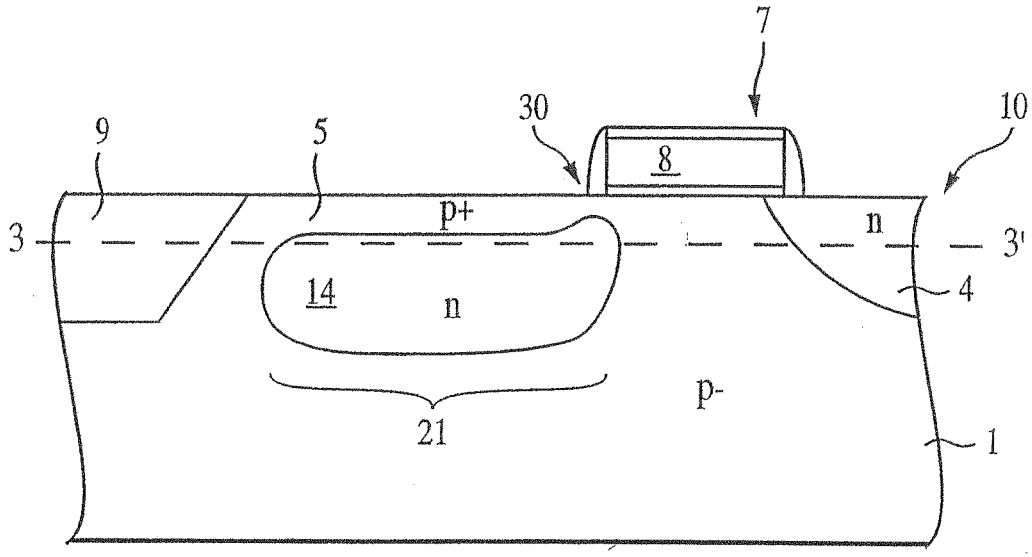


FIG. 2
PRIOR ART

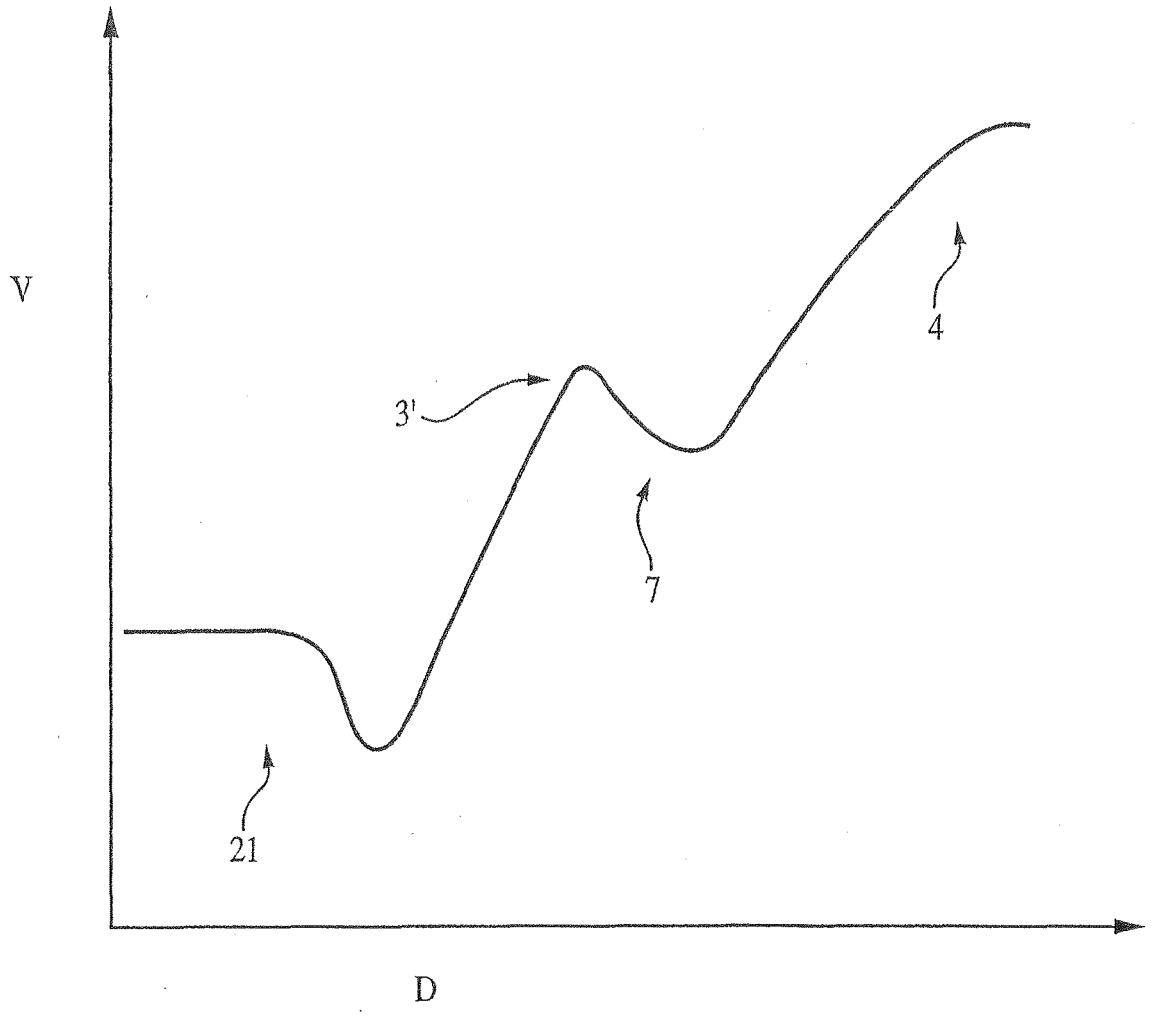


FIG. 3
PRIOR ART

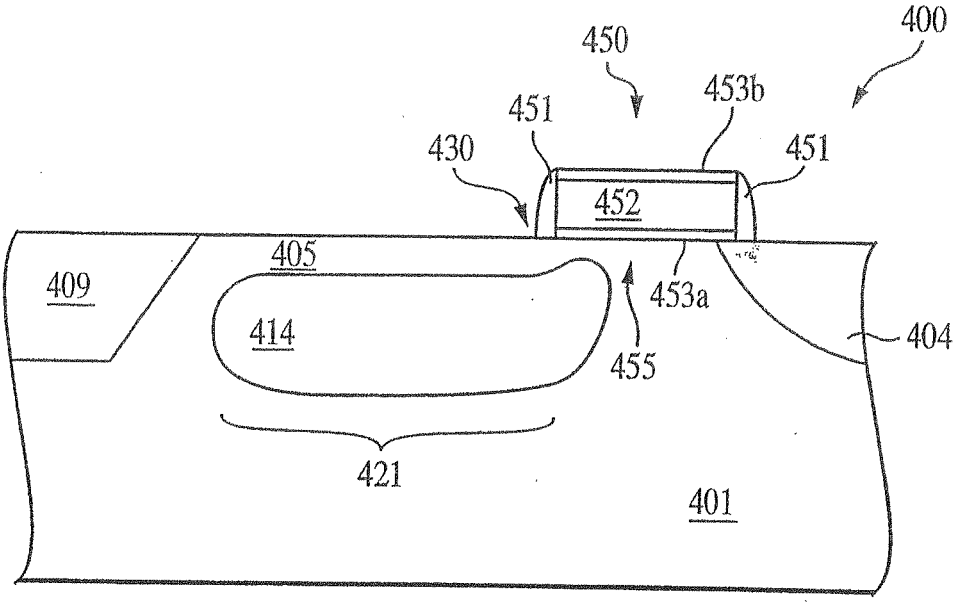

400
450
451
453b
430
451
452
405
409
453a
414
404
455
421
401

FIG. 4

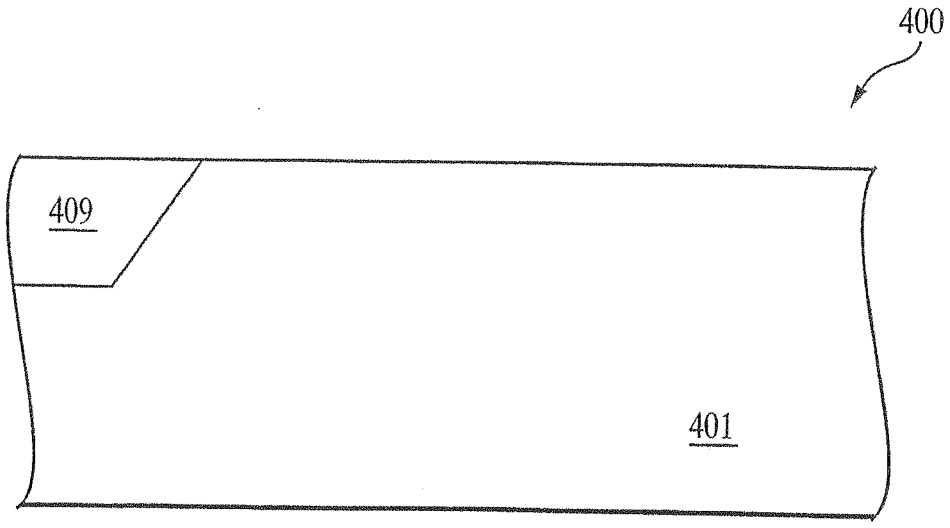

400
409
401

FIG. 5A

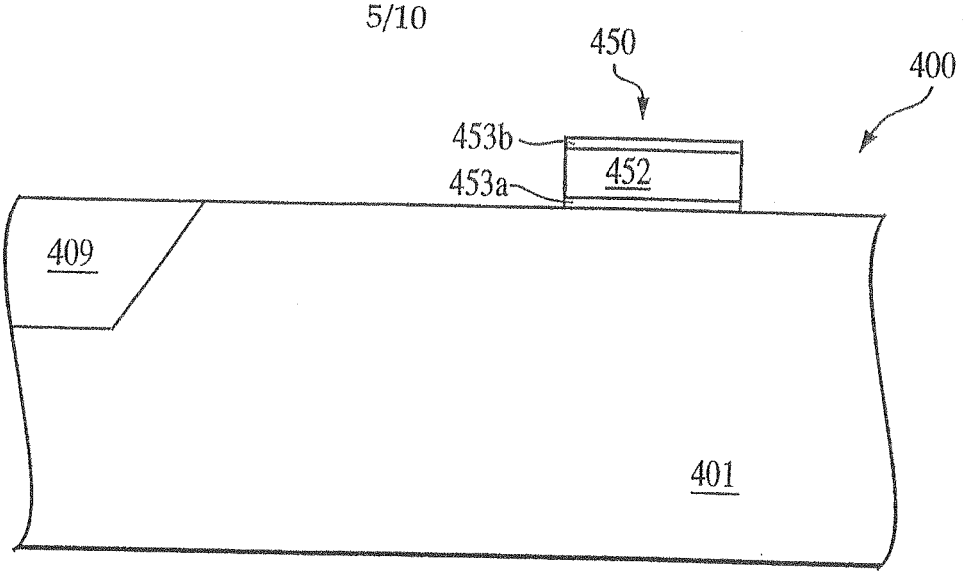

450
400
453b
452
453a
409
401

FIG. 5B

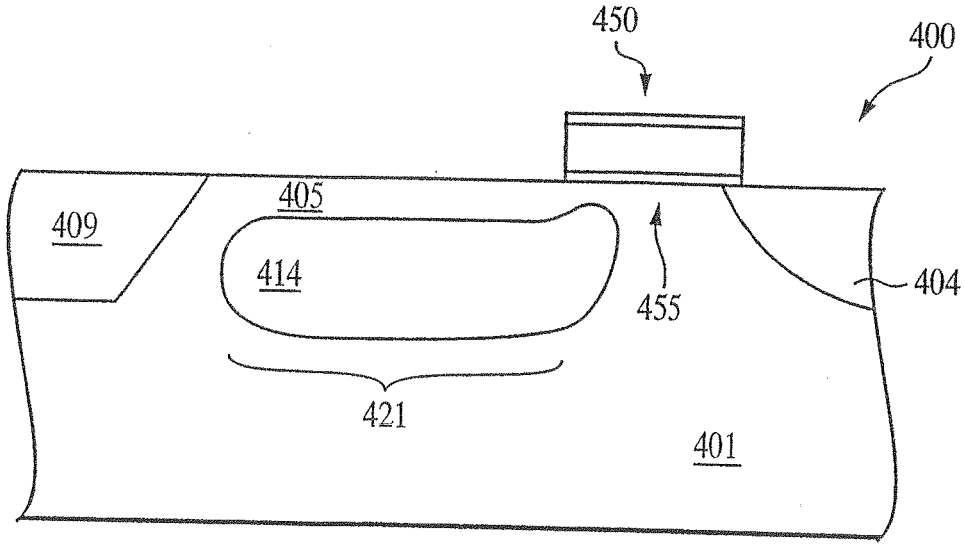

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400
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409
414
455
404
421
401

FIG. 5C

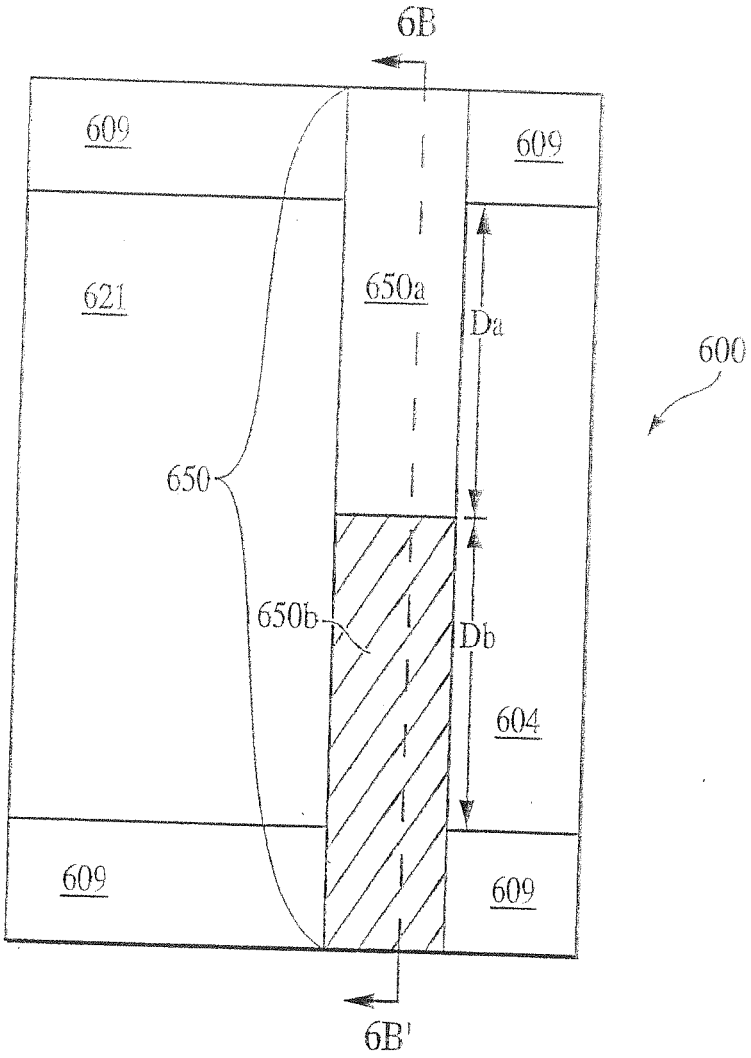

6B
609
609
621
650a
Da
600
650
650b
Db
604
609
609
6B'

FIG. 6A

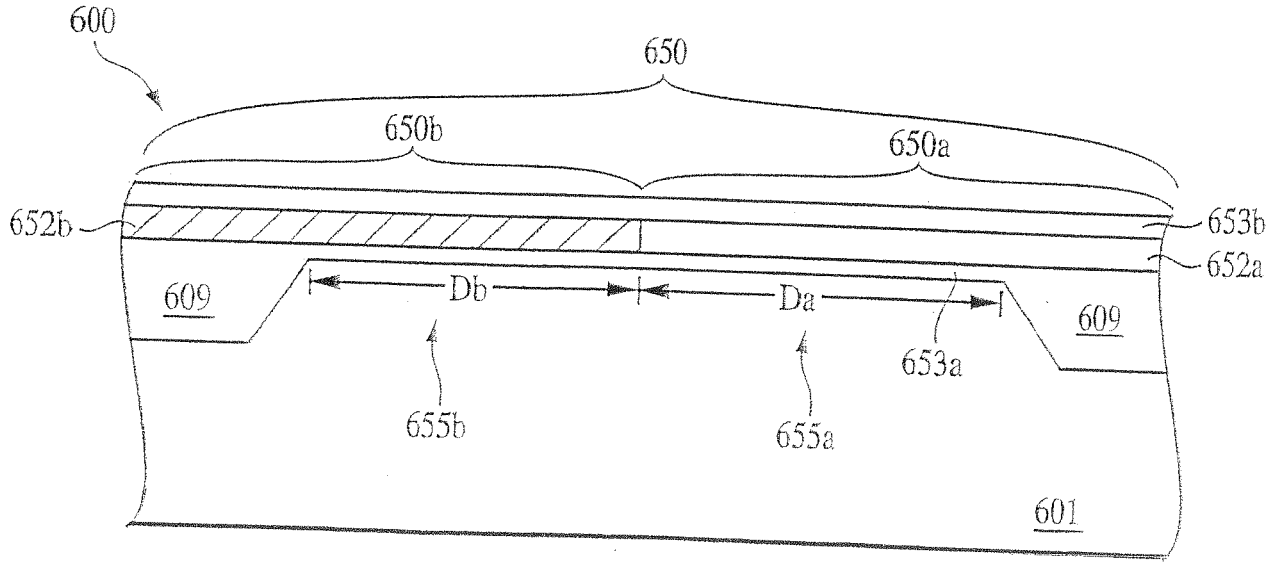

600
650
650b
650a
652b
653b
652a
609
Db
Da
609
653a
655b
655a
601

FIG. 6B

WO 2005/004240 PCT/US2004/020010

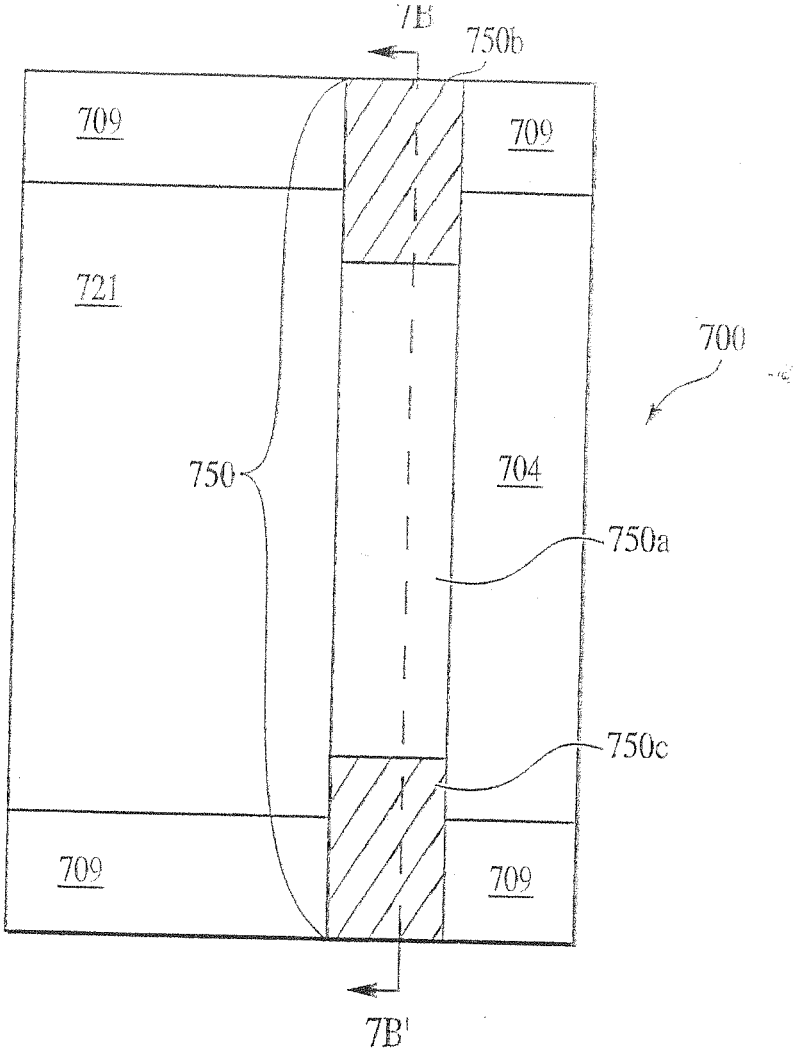


FIG. 7A

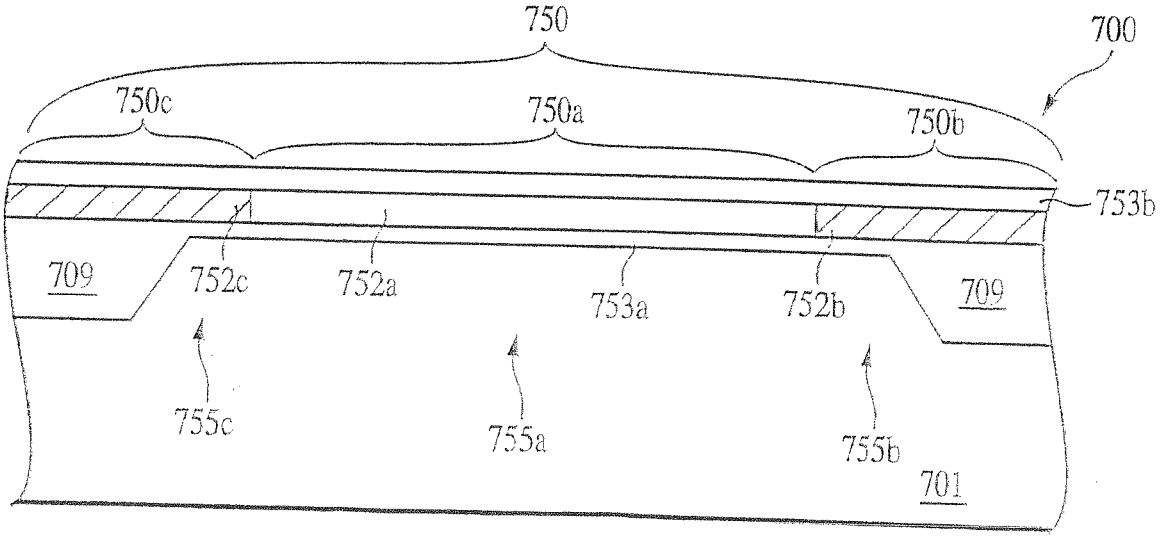


FIG. 7B

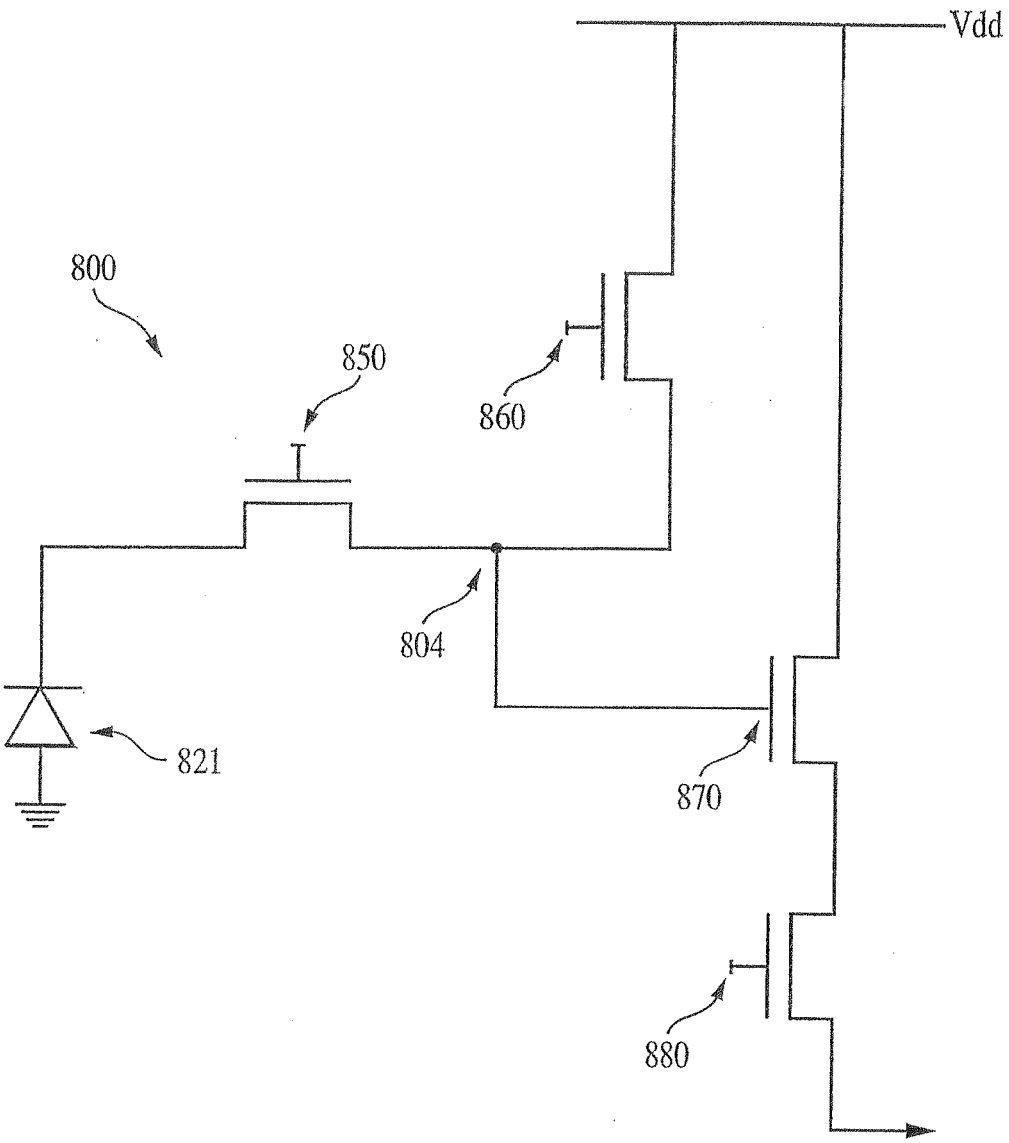


FIG. 8

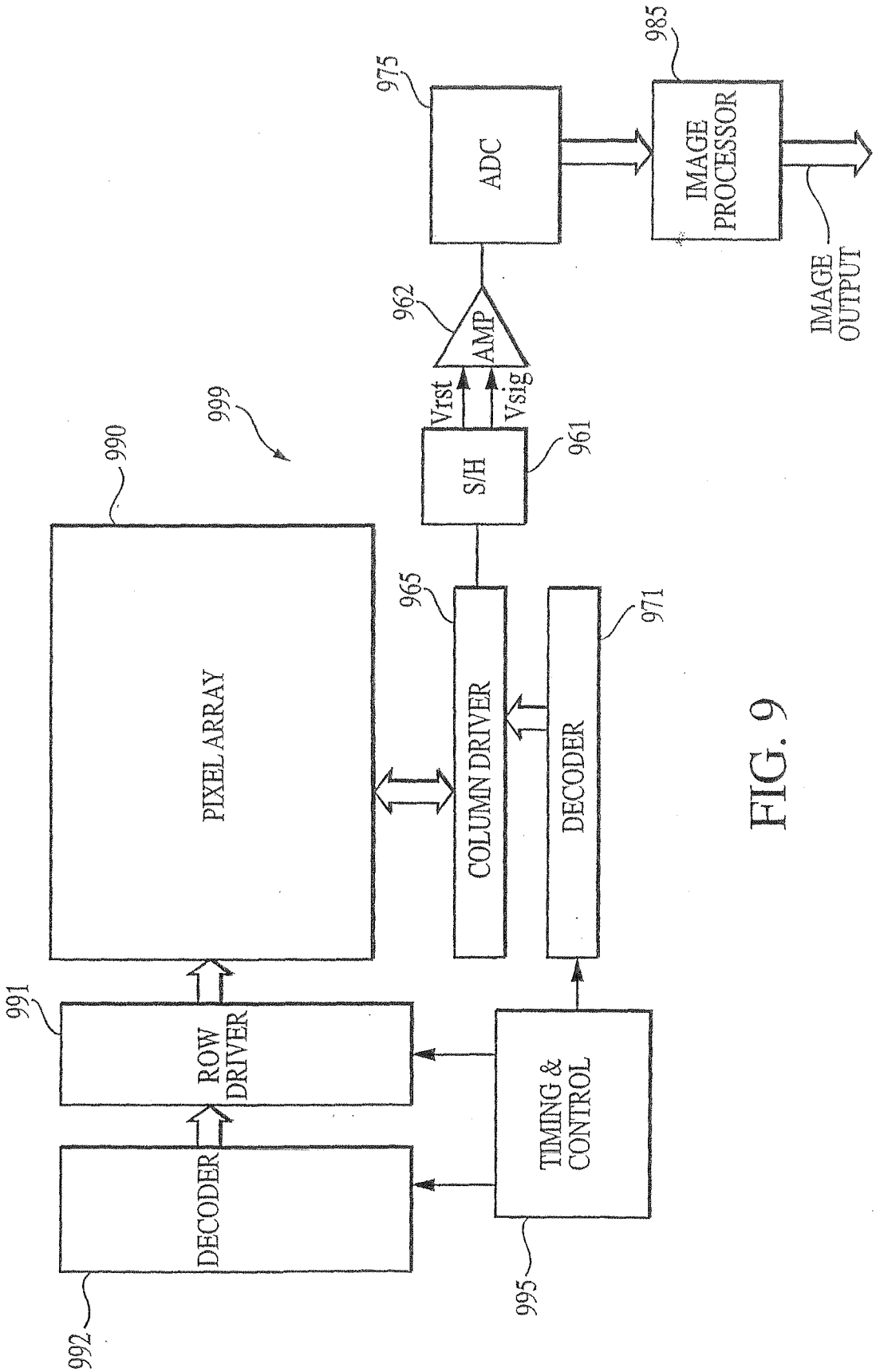

985
975
ADC
IMAGE PROCESSOR
IMAGE OUTPUT
962
AMP
Vrst
Vsig
999
990
S/H
961
965
971
PIXEL ARRAY
COLUMN DRIVER
DECODER
991
ROW DRIVER
TIMING & CONTROL
DECODER
995
992

FIG. 9

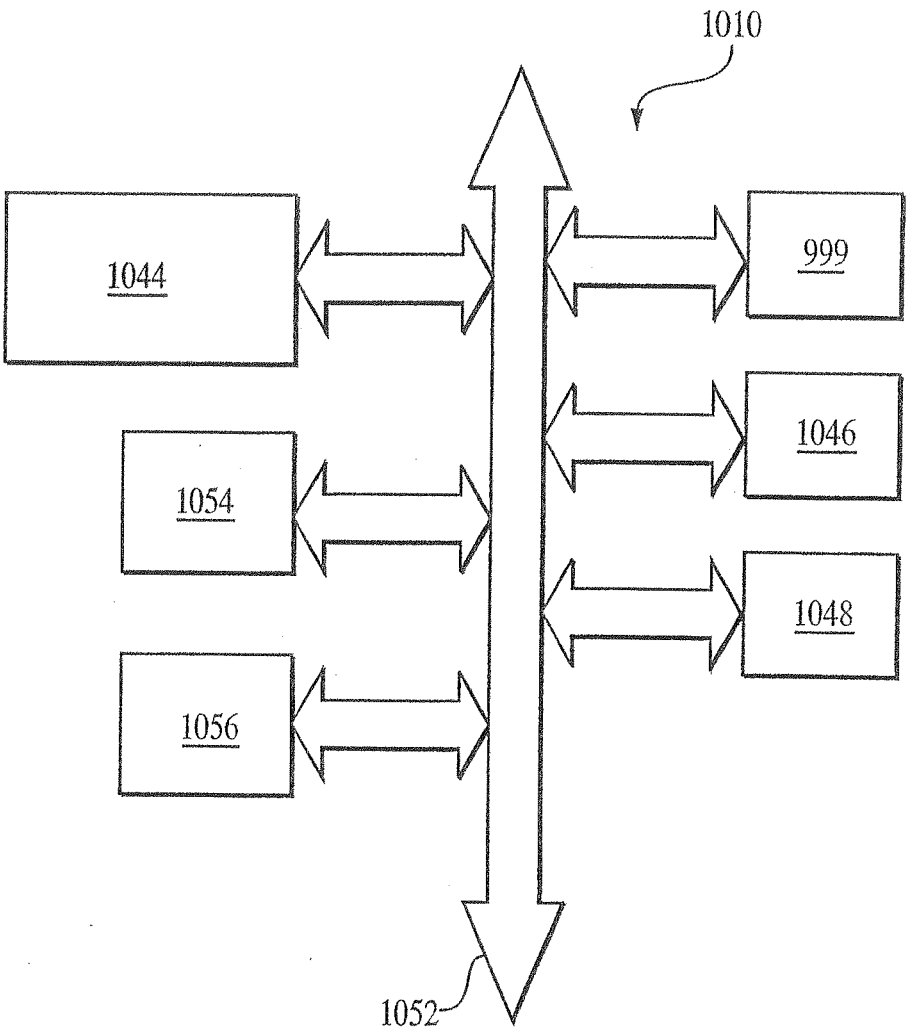


FIG. 10