RAPID THERMAL ANNEALING OF SILICON STRUCTURES

FIELD OF INVENTION

The present invention relates to rapid thermal annealing (RTA) in the fabrication of semiconductor devices and particularly, but not exclusively, to the use of RTA to reduce defects in high density metal oxide semiconductor field effect transistor (MOSFET) devices.

BACKGROUND

In the fabrication of semiconductor devices the likelihood of defects or dislocations increases as the dimensions of elements in the devices, and the distance between adjacent elements, becomes smaller and is insufficient to allow for tolerances in manufacturing processes. Examples of such processes include photo-lithographic masking, ion implantation, and thermal process steps in which volume changes are thermally generated.

Figure 1 shows some of the steps of a known semiconductor fabrication process by which a MOSFET semiconductor device using shallow trench isolation (STI) may be manufactured. One example MOSFET device is shown in Figure 2. Shallow isolating trenches 21 are formed in a STI formation step 1. An ion implantation step 2 forms wells 22. Gates 23 and lightly doped drain regions 24 are formed by a further ion implantation step 3. These implantation steps 32, 33 are performed subsequent to formation of the isolating trenches 21. Nitride spacers 26 are formed in process step 5 and source/drain regions 27 are formed in an ion implantation step 6.

The implantation steps create nucleation sites which increase stresses 25 occurring at the corners of the trenches and contribute to the generation of dislocations and defects under the influence of subsequent thermal steps. These defects can be a problem particularly in dense memory areas.

Where trench depth is not large enough, peak stress points at the upper and lower corners of the trenches can be close to the dislocation sites generated during implantation.

As individual MOSFET devices are scaled down in size to achieve higher densities on a wafer, the margins between device elements decrease, the likelihood that adjacent stresses and dislocations will interfere increases, and the probability of a higher number of resulting defects on a wafer increases.

The increased number of these defects and dislocations can generate high device leakage currents.

These problems can be mitigated to some extent by the use of a rapid thermal annealing step 4 performed after the implantation of the gate and lightly doped drain regions in step 3 and performed again, in step 7, after the implantation of the source/drain regions in step 6. These known RTA process steps 4, 7 are performed in an inert atmosphere, typically nitrogen.

The use of these known annealing steps is not sufficient to eliminate the defects and dislocations, particularly in high density structures. High leakage currents can still occur in these cases.

J-w. Jung, J-S. Roh, Y. Lee, and K. Lee, "Two-Step Rapid Thermal Annealing (TS-RTA) to Suppress Out-Diffusion of Dopants without Degrading Short Channel Effect of Transistor," IEEE Electron Device Lett, vol. 21, pp. 376-377, Aug. 2000 describes activation of dopants in the source/drain and gate of MOSFET devices by experimental annealing processes. In a TS-RTA process, samples were successively annealed at 700 ^{O}C for 3 minutes in oxygen gas and then at 1000 ^{O}C for 40 seconds in nitrogen gas. In a one-step RTA (OS-RTA) process, samples were annealed at 1000 ^{O}C for 30 seconds in nitrogen gas or in a mixture of oxygen and nitrogen gases.

In Jung *et al*, the resistance of n-type poly-silicon was said to increase with the annealing time in the OS-RTA process and only the TS-RTA process was said to effectively prevent out-diffusion of arsenic ions without degrading the short channel effect (SCE).

SUMMARY OF INVENTION

It is an object of one embodiment of the invention to provide a one-step annealing process which goes at least some way toward mitigating some of the problems of the prior art.

In a first aspect the invention may be broadly said to be a single-step rapid thermal annealing (SS-RTA) process by which a semiconductor material is annealed, the single process step including annealing the semiconductor material at an elevated temperature for a predetermined time in an atmosphere comprising substantially oxygen gas in the absence of any other gas.

The semiconductor material may be polycrystalline silicon.

Preferably the atmosphere is substantially free of nitrogen.

Preferably the elevated temperature is substantially in the range from $900^{O}C$ to $1100^{O}C$.

Preferably the predetermined time is substantially in the range from 20 to 40 seconds.

In a second aspect the invention may be broadly said to be a method of fabricating a metal oxide semiconductor field effect transistor (MOSFET), the method including the SS-RTA process of the first aspect.

In a third aspect the invention may be broadly said to be a method of reducing the leakage current in a high-density memory area in a semiconductor device, by annealing the device during fabrication of the device using the SS-RTA process of the first aspect.

In a fourth aspect the invention may be broadly said to be a method of reducing defects created during fabrication of a semiconductor device, the method including the SS-RTA process of the first aspect.

In a fifth aspect the invention may be broadly said to be a MOSFET device, fabricated using the SS-RTA process of the first aspect.

In a sixth aspect the invention may be broadly said to be a semiconductor device including a high-density memory area, the device being annealed during fabrication of the device using the SS-RTA process of the first aspect.

The invention may further be said to consist in any alternative combination of process steps mentioned herein. Known equivalents of such steps which are not expressly set out are nevertheless deemed to be included.

BRIEF DESCRIPTION OF DRAWINGS

Preferred forms and methods of the invention will be further described, by way of example only and without intending to be limiting, with reference to the accompanying figures of which;

Figure 1 shows part of a prior art process for fabrication of semiconductor devices,

Figure 2 shows a semiconductor device which may be made using the fabrication steps shown in Figures 1 and 3, and

Figure 3 shows part of a process for fabrication of semiconductor devices in accordance with the current invention.

DETAILED DESCRIPTION OF PREFERRED FORMS

A RTA process according to the present invention has application in the fabrication of semiconductor devices such as MOSFETs based on polycrystalline silicon (poly-silicon) wafers and particularly in the fabrication of such devices in high-density memories.

A typical MOSFET construction fabricated using shallow trench isolation (STI) is shown in Figure 2. The MOSFET includes a shallow isolating trench 21, well 22, poly-silicon gate 23, lightly doped drain 24, nitride spacer 26, and source/drain region 27. As explained above, such a device, when made with a known method using the steps shown in Figure 1, can include defects such as the stresses 25 occurring at corners of the isolation trenches. These stresses are increased by nucleation sites created during the ion implantation steps. With shallow trench depths, the upper and lower corners of the trenches are close to dislocation sites generated during implantation. These defects can be annealed out, or at least reduced, by using the SS-RTA process in accordance with the current invention.

Figure 3 shows part of a process using the current invention and by which MOSFET devices, for example that shown in Figure 2, may be fabricated. Shallow isolating trenches 21 are formed in a STI process step 31. An ion implantation step 32 forms wells 22. Gates 23 and lightly doped drain regions 24 are formed by a further ion implantation step 33.

As explained above, the implantation steps 32, 33 create nucleation sites which increase stresses 25 occurring at the corners of the isolation trenches 21 and contribute to the generation of dislocations and defects. These can be eliminated or at least mitigated to some extent by annealing the wafer using the SS-RTA process according to the invention and shown as process step 34.

In the SS-RTA step 34, the wafer is annealed for a duration of between 20 and 40 seconds in an atmosphere of oxygen at a temperature between 900 ^{O}C and 1100 ^{O}C. The oxygen atmosphere is substantially free of other gases and particularly is free of nitrogen.

Nitride spacers 26 are then formed in process step 35 and source/drain regions 27 formed in an ion implantation step 36.

After creation of the spacers and implantation of the source/drain regions, defects caused by this implantation are annealed by repeating the SS-RTA process in step 37.

The SS-RTA process anneals out the defects created or generated during prior implantation or through volume expansion due to subsequent thermal budget by diffusing oxygen through the silicon to form oxides and passivate the defects.

The SS-RTA process of the present invention also reduces out-diffusion of ions, e.g. boron and arsenic, by oxidizing the wafer surface. The SS-RTA process also reduces transient enhanced diffusion (TED) effects and thereby reduces variation in the threshold voltage (V_{th}) in short channel structures. It also reduces the overall device leakage current (I_{DDQ}) which is particularly helpful in low leakage application devices.

The SS-RTA process of the present invention is not limited to any particular layout or topography but is particularly advantageous in advanced technology devices having high density topographies where the dimensions of active elements, and the spaces between the elements, are very small. Such devices have a higher probability of an increased number of defects per unit area. Typical of such devices are those having high density memory areas, such as flash memory or static random access memory (SRAM).

CLAIMS

1. A method of fabricating a metal oxide semiconductor device, wherein said device uses shallow trench isolation (STI), said method including performing the following steps in order:

forming shallow isolating trenches;

at least one ion implantation step to form wells, gates and lightly doped drain regions; and

annealing said metal oxide semiconductor device at an elevated temperature for a predetermined time in an atmosphere comprising substantially oxygen gas in the absence of nitrogen.

2. A method of fabricating a metal oxide semiconductor device, as claimed in claim 1 wherein said metal oxide semiconductor device is a metal oxide semiconductor field effect transistor.

3. A method of fabricating a metal oxide semiconductor device as claimed in claim 1 or claim 2, wherein said device includes polycrystalline silicon wafers.

4. A method of fabricating a metal oxide semiconductor device as claimed in one of the preceding claims, wherein the atmosphere is substantially free of any gas other than oxygen.

5. A method of fabricating a metal oxide semiconductor device as claimed in one of the preceding claims, wherein the elevated temperature is substantially in the range from 900 to 1100°C.

6. A method of fabricating a metal oxide semiconductor device as claimed in one of the preceding claims, wherein the predetermined time is substantially in the range from 20 to 40 seconds.

7. A method of reducing the leakage current in a high-density memory area in a semiconductor device, comprising fabricating the device using the method as claimed in any one of claims 1 to 5.

8. A method of reducing defects created during fabrication of a semiconductor device, comprising fabricating the device using the method as claimed in any one of claims 1 to 5.

9. A metal oxide semiconductor field effect transistor (MOSFET) device fabricated using the method as claimed in any one of claims 1 to 5.

10. A semiconductor device including a high-density memory area, fabricated using the method as claimed in any one of claims 1 to 5.

11. A method of fabricating a metal oxide semiconductor field effect transistor, wherein said transistor uses shallow trench isolation (STI), said method including performing the following steps in order:

forming shallow isolating trenches;

at least one ion implantation step to form wells, gates and lightly doped drain regions; and

annealing said metal oxide semiconductor field effect transistor at a temperature in the range from 900 to 1100°C.for 20 to 40 seconds. in an atmosphere comprising substantially oxygen gas in the absence of nitrogen or any other gas,

wherein said transistor includes polycrystalline silicon wafers