

A SEMICONDUCTOR DEVICE IN A THIN ACTIVE LAYER WITH HIGH BREAK-DOWN VOLTAGE

TECHNICAL FIELD

The present invention relates to a semiconductor device in a
5 thin active layer with high breakdown voltage, said device
having charge carrier depleted regions of reduced electrical
field strength and comprising

- a semiconductor body;
 - a component region of semiconductor material carried by the
10 semiconductor body and having an upper surface which region is
weakly doped with a first type (n) of doping material;
 - a dielectric isolating layer which delimits a lower surface
of the component region from the semiconductor body;
 - an electrically delimiting separation layer which extends
15 along the remaining surfaces of the component region that
border on the semiconductor body;
 - a sunken region in the component region that has a relatively
low concentration of a second type (p) of doping material
which is opposite to the first type of doping material,
20 wherein the sunken region extends from the upper surface of
the component region;
 - a PN-junction at the surface of the sunken region that
delimits said region from a remaining part of the component
region;
 - 25 - at least one semiconductor component in the component
region; and
 - at least two electrical connections in the component
region, wherein the regions of reduced electrical field
strength are depleted of charge carriers by electrical
30 voltages applied to the electrical connections and a first of
the charge carrier depleted regions extends from the PN-
junction to the dielectric isolating layer, at least beneath
a part of the sunken region.
- 0-4212080

BACKGROUND ART

Semiconductor circuits are required to withstand a relatively high voltage in many different kinds of applications. An example of one such application is found in the subscriber
5 line circuits of telephone exchanges. In older Swedish telephone exchanges, the line to a subscriber was required to have an applied voltage of 48 volts, and modern subscriber line circuits in semiconductor techniques are adapted to these voltages. Higher voltages are required in other countries, for
10 instance 68 volts in Germany, while other applications of semiconductor circuits may use still higher voltages, for instance voltages of 400 volts or more.

One problem with these relatively high voltages is that the electrical field strength may exceed the critical field
15 strength of the semiconductor material in certain regions of a component. This can result in a current breakthrough which destroys the semiconductor material if the current is not limited. The same problem of high field strength also occurs in very small and rapid semiconductor components intended for
20 calculating or computing circuits. Although these components are connected to low voltages, in the order of 3 to 5 volts, the small extensions of the components enable the electrical field strength to reach high values.

In certain applications, the problem of high electric field
25 strength is pronounced at the surface of a semiconductor component, as described in an article in IEEE, Proceedings from IEDM, 1979, pages 238-241, by J.A. Appels and H.M.J. Vaes: "High Voltage Thin Layer Devices (Resurf Devices)", this article being herewith incorporated in the present descrip-
30 tion. The semiconductor component has a surface layer in which there is included a PN-junction in which the critical field strength of the material is reached at a given applied voltage. The surface layer is weakly doped on one side of the

PN-junction and this weakly doped part can be depleted of charge carriers by making the surface layer relatively thin. The applied voltage is herewith distributed over a long distance along the component surface, so that the maximum
5 field strength will adopt a value beneath the breakdown field strength. The phenomenon is well known within semiconductor technology and has been given the personal acronym RESURF (REduced SURface Field). The resurf technique is described in more detail in an article in Philips J. Res. 35, 1-13, 1980,
10 J.A. Appels, et al: "Thin Layer High-Voltage Devices". This article is also incorporated in the present description.

The U.S. Patent Specification 4,409,606 describes the resurf technique applied to a transistor. A relatively thin semiconductor layer in which the transistor is formed is mounted on
15 a semiconductor substrate. The substrate and the layer form a PN-junction and a heavily doped region in the PN-junction is arranged beneath one transistor connection. This junction is reverse biased and the thin semiconductor layer is depleted of charge carriers up to the layer surface, along a path which
20 extends between the heavily doped region and the second transistor connection. A good degree of safety against current breakthrough is obtained when this path is made sufficiently long. Such application of the resurf technology deals with those problems that occur with breakdown voltage at the base
25 of a bipolar transistor due to current amplification, often referred to as common base amplification and designated α_0 in the literature. A similar arrangement is also described in U.S. Patent Specification 4,639,761.

The European Patent Application No. A1-0,086,010 describes a
30 transistor which is similar to the transistor described in the two aforesaid U.S. patent specifications. This latter transistor, however, lacks the heavily doped region in the PN-junction, and the layer in which the transistor is formed has an elevated doping concentration. It is therefore difficult

to fully deplete this layer of charge carriers and an isolated electrode is placed over those regions to be depleted of charge carriers in order to achieve total depletion.

In the case of the two aforesaid U.S. patent specifications
5 and the European patent application, the transistor is connected to the semiconductor substrate of the device through the aforesaid PN-junction. The transistor is delimited laterally by deep, heavily doped regions which have reverse-biased PN-junctions. One drawback with the thus delimited
10 transistors is that they take up a large amount of space in the substrate. This drawback is avoided with an arrangement according to European Patent Application No. A1-0,418,737, which describes transistors on a common substrate that are dielectrically isolated from one another. A surface of a
15 semiconductor substrate is oxidized to form an isolating layer on which a relatively thin wafer of epitaxial semiconductor material is mounted. This epitaxial wafer has etched therein grooves which extend down to the isolating layer. The side surfaces of the grooves are oxidized and the grooves filled
20 with polycrystalline semiconductive material. Components are formed in the dielectrically isolated, box-like regions thus formed. These components have an external connection which is connected to a heavily doped connecting layer beneath respective components on the box bottom, in direct abutment with the
25 isolating oxide layer.

The European Patent Application No. A2-0,391,056 describes an alternative method of forming a semiconductor substrate with dielectrically isolated regions. The isolated regions are produced by repeatedly etching the substrate and coating with
30 semiconductor material. The dielectric isolation is comprised of oxidized semiconductor material. The regions have a weakly doped area in which the actual component is formed and a heavily doped connection layer which is located beneath said

component and lies against the dielectrically isolating layer.

The three U.S. Patent Specifications No. 4,587,545, No. 4,587,656 and No. 4,608,590 teach high voltage semiconductor switches. The switches are gate-provided diodes which are formed in a dielectrically isolated region of relatively weakly doped semiconductor material. An anode and a cathode are diffused into the surface of the isolated region and the electrical connection therebetween can be broken with the aid of a gate in the surface of said region. The anode and the cathode have a type of doping which is opposite to the type of doping of the isolated region. The regions around the anode and the cathode can be depleted of charge carriers in accordance with the resurf technique, by applying appropriate voltages to the switch, which thereby becomes highly resistive in its cut-off state.

DISCLOSURE OF THE INVENTION

In accordance with the invention, this patent document pertains to an application of the known resurf technique in an electrically delimited component region for a class of components that differ from earlier disclosed classes of components in corresponding delimited regions. More specifically, the invention includes a bipolar transistor connected in series with a field effect transistor. This transistor arrangement is formed in a component region which has a dielectrically isolated layer at its bottom surface. The bipolar transistor has a base region which extends downwardly from the upper surface of the component region. A PN-junction between the base region and the component region delimits said base region and can be reverse biased so that a region between the base region and the dielectrically isolating layer is depleted of charge carriers. This depletion occurs at a collector voltage of some few volts and can be readily

achieved because the component region is relatively weakly doped and because the depleted region beneath the base region is significantly much thinner than in the case of known bipolar transistors. Despite the thinness of this region
5 beneath the base region, the transistor device is able to withstand high voltages due to the fact that the voltage is taken-up laterally by the component region beneath the charge carrier depleted base region. The transistor device has a series resistance which is normal for bipolar transistors,
10 which is unexpected in view of the fact that the device lacks a highly doped collector region beneath the base region. The characteristics of the transistor device are also in good accord with corresponding earlier known characteristics. The inventive transistor device is significantly thinner than
15 corresponding known devices and takes up a much smaller area on its semiconductor substrate than these earlier known devices.

The invention is characterized by the features set forth in the following Claims.

20 BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described in more detail with reference to exemplifying embodiments thereof and also with reference to the accompanying drawings, in which
Figure 1 is a cross-sectional view of a bipolar transistor
25 and a field effect transistor;
Figure 2 is a cross-sectional view showing field lines of the transistors illustrated in Figure 1;
Figure 3 is a schematic illustration of the transistors in Figures 1 and 2;
30 Figure 4 is a schematic illustration of two series-connected transistors;
Figure 5 is a cross-sectional view of the transistors in Figure 4;

- Figure 6 is a view of the transistors in Figure 5 from above;
 Figure 7 is a cross-sectional view showing field lines relating to the transistors in Figure 4;
 Figure 8 is a view showing field lines relating to the transistors in Figure 4, as seen from above;
 Figure 9 illustrates a current-voltage characteristic of the transistor device in Figure 1;
 Figure 10 is a diagram showing comparison curves relating to a known and to an inventive transistor; and
 Figures 11 to 14 are cross-sectional views illustrating the different stages of manufacture of the transistors shown in Figure 1.

BEST MODE OF CARRYING OUT THE INVENTION

- Figure 1 is a cross-sectional view of an inventive bipolar NPN transistor BIP1 which is connected in series to a field effect transistor JFET1. A semiconductor substrate 1, in this case a silicon substrate, has an upper surface which is oxidized to form an electrically isolating silicon-dioxide layer 2. A relatively thin wafer 3 of monocrystalline silicon is mounted on the upper layer 2, this wafer being the active layer of the transistor device BIP1 and JFET1. The active layer has a relatively low concentration of negative charge carriers, referenced n in the Figure. The monocrystalline wafer 3 has a thickness A_1 which in the case of the illustrated embodiment is equal to $4\ \mu\text{m}$. A component region 4 is delimited against surrounding parts 4a and 4b in the wafer 3, by means of a separation layer 5 comprised of silicon dioxide and polycrystalline silicon. The separation layer 5 extends from the surface of the monocrystalline wafer 3 down to the isolating layer 2 and fully surrounds the transistors BIP1 and JFET1. The component region 4 is hereby totally isolated electrically from the substrate 1 and the surrounding parts 4a and 4b of the monocrystalline wafer 3.

The transistor BIP1 has a base region B which is doped with positive charge carriers referenced p in the Figure. The base B has a connection region B1 for coaction with an external electrical connection, this connection region being heavily doped p^+ with positive charge carriers. The base region B of the transistor BIP1 includes an emitter E1 which is heavily doped n^+ with negative charge carriers. A collector region K1 of the transistor BIP1 is also located in the component region 4. A gate connection G1 of the transistor JFET1 is common with the base connection B1 and a source region S1 of said transistor is common with the collector region K1 of the transistor BIP1. A heavily n^+ doped region D1 forms the drain connection of the transistor JFET1.

The component region 4 is covered by a silicon-dioxide isolating layer 6, which is provided with openings 7 for external electrical connections 8. These connections are connected to respective connection regions B1 of the base, the emitter E1 and the drain region D1. The configuration of such external electrical connections is well known and the connections have not been shown in detail in Figure 1, so as not to complicate the Figure unnecessarily.

Figure 3 is a schematic illustration of the series-connected transistors BIP1 and JFET1. The base connection B1 is connected to the gate connection G1 and the collector K1 is connected to the source region S1. Each of the base connection B1, the emitter E1 and the drain connection D1 has one of the external connections 8.

In a typical operational case, the transistors BIP1 and JFET1 are connected to the following voltages:

- 30 Drain voltage $V_D = +70 \text{ V}$
- Emitter voltage $V_E = 0 \text{ V}$ (earth)
- Base and gate voltage $V_B = 0.6 \text{ V}$

The transistor BIP1 has a PN-junction 9 at the bottom surface of the base region B which is reverse biased and depleted of charge carriers in a typical manner through the voltages applied. In accordance with the invention, a region DP1
 5 between the PN-junction 9 and the isolating layer 2 is relatively weakly doped and also has a relatively small thickness $A_2 = 2 \mu\text{m}$. The entire region DP1 is therefore depleted of charge carriers and a large part of the electric voltage between the base region B and the drain region D1 is
 10 distributed over a relatively long path L. As a result, an electric field strength E_D in the depletion region DP1 assumes a low value, all in accordance with the resurf technique as presented in the two aforesaid references "High Voltage Thin Layer Devices" by J.A. Appels and H.M.J. Vaes, and "Thin Layer
 15 High-Voltage Devices" by J.A. Appels, et al. The field strength in the region DP1 can be kept beneath the critical field strength E_{CR} of the silicon, which is about $3 \cdot 10^5 \text{ V/cm}$, preventing a surge of current I in this region.

It should be carefully noted that the entire region DP1 in the
 20 inventive transistor BIP1, right down to the isolating layer 2, is comprised of weakly doped material which is easily depleted of charge carriers. Many known transistors include a highly doped layer placed beneath the base region of the transistor, a so-called buried layer, in distinction to the
 25 aforesaid, and there is a long distance between the PN-junction of the base region and this highly doped layer, so that the known transistor is able to withstand high voltages. A corresponding highly doped layer would completely destroy the resurf effect in the inventive transistor device BIP1 and
 30 JFET1 in Figure 1. A highly doped layer is difficult to deplete of charge carriers and the electrical field strength of such a contemplated layer would reach the breakdown field strength E_{CR} at a relatively low voltage between the drain region D1 and the emitter E1. The region D1 is depleted of
 35 charge carriers at a drain voltage V_D of only some few volts.

Figure 2 illustrates an enlarged part of Figure 1. The Figure illustrates the isolating layer 2, part of the component region 4, part of the base region B with the connection region B1 and G1 and the emitter E1, the drain region D1 and a part of the depleted region DP1. Figure 2 also includes a family of curves C related to the electrical field E_D . The curve family includes curves identified by digits $0.5 \cdot 10^5$, $1 \cdot 10^5$... $2.5 \cdot 10^5$ and the electrical field strength along a curve has a constant value. This value is given by the digit sign for respective curves and has been given in the unit volt/cm, so that, for instance, the field strength along the curve farthest to the left in the Figure has the value $0.5 \cdot 10^5$ V/cm. The field strengths appear when the component is connected to the aforesaid operational voltages. The curve family C is based on an arithmetic model which experience has shown to produce very precise values. It will be seen that the electrical field strength in the depletion region DP1 is low, so as to prevent surging of the current I. It will also be seen that the electrical field E_D has a relatively high field strength at the surface of the component region 4, in the vicinity of the isolating layer 6. At normal voltages of the transistors BIP1 and JFET1, practically no current will flow in this part of the component region 4 and neither will current surges occur. However, the relatively high field strength limits the voltages that can be applied to the transistor device BIP1 and JFET1.

In the case of the Figure 1 embodiment, the component region 4 is surrounded by the separation layer 5, which is dielectrically isolating. In the case of an alternative embodiment, the separation layer is comprised of a heavily and positively p^+ -doped region which surrounds the component region 4 and extends from the surface of the monocrystalline layer 3 down to the dielectrically isolating layer 2. The separation layer has a PN-junction to which a reversed voltage is applied so as

to delimit the component region 4 electrically against the surrounding parts 4a and 4b.

An alternative embodiment of the invention will now be described with reference to Figure 4, Figure 5 and Figure 6.

5 Figure 4 illustrates schematically a bipolar transistor BIP2 which is connected in series to a field effect transistor JFET2. The transistor BIP2 has an emitter E2 and a base B2 which is connected to a gate G2 of the field effect transistor JFET2. This transistor has a drain connection D2 and also a

10 source connection S2, which is connected to a collector K2 of the transistor BIP2.

Figure 5 is a cross-sectional view of one embodiment of the transistors BIP2 and JFET2. The cross-section is taken on the line A-A in Figure 6. The upper surface of a silicon substrate

15 21 is oxidized to form an isolating layer 22, and a weakly n-doped monocrystalline wafer 23 is mounted on the layer 22. The wafer 23 has a thickness of 4 μm , similar to the earlier embodiment. A component region 24 is delimited in the monocrystalline wafer 23 by a separation layer 25 which surrounds the

20 component region 24. The separation layer is comprised of trenches in the mono-crystalline wafer 23, the sides of which are oxidized to form electrically insulating layers and the remainder of the trenches is filled with polycrystalline silicon. The component region 24 is hereby isolated electrically

25 from surrounding parts 24a and 24b of the monocrystalline wafer 23. The bipolar transistor BIP2 and the field effect transistor JFET2 are arranged in the component region 24. In order not to complicate the Figure unnecessarily, protective surface layers with openings for external connections

30 26 have not been shown in the Figure. The connections 26 are only shown schematically.

The transistor BIP2 has a base region B3 which is positively p-doped relatively weakly and has a heavily positively p⁺-

doped connection region B2. The emitter E2 of the transistor BIP2 is located in the base region B3 and is heavily n^+ -doped. The base region B3 extends from the upper surface of the component region 24 down to a PN-junction 29 at the underside of the base region B3. Located between the PN-junction 29 and the isolating layer 22 is a region DP2 which is uninfluenced by the doping of the base region. The collector region K2 of the transistor BIP2 is located on one side of the base region B3, as shown in the Figure, by a chain line. With the embodiment of the invention illustrated in Figure 5, high electric field strengths are avoided in the whole of the collector region K2, as will be described in more detail herebelow.

The gate connection G2 of the transistor JFET2 is common with the base connection B2. The active gate itself is comprised of two p-doped regions G3 which project out from the base region B3 in the form of bifurcate projections which extend along the sides of the separation layer 25. The configuration of the gate region is shown more clearly in Figure 6, which illustrates the transistors BIP2 and JFET2 from above. Figure 5 illustrates the gate region G3 in broken lines. The case of the illustrated embodiment, the bifurcate projections G3 extend down into the component region 24 to the same depth as the base region B3, but may extend right down to the isolating layer 22. The source region S2 of the transistor JFET2 is common with the collector region K2 of the transistor BIP2. The drain connection D2 of the transistor JFET2 is comprised of a heavily and negatively n^+ -doped region.

Figure 6 illustrates the different regions of the transistors BIP2 and JFET2 from above. The component region 24 is completely surrounded by the separation layer 25 and the base region B3 extends transversely across the elongated component region in one end of said region. The base connection B2 and the emitter connection E2 are comprised of elongated regions which

extend in the transverse direction of the component region 24. The bifurcate projections G3 projecting from the base region B3, the gate of the transistor JFET2, extend in the longitudinal direction of the component region 24 along the separation layer 25 and along a respective side of the component region. The drain connection D2 is positioned at the other end of the component region. The Figure also illustrates an alternative embodiment of the gate connection G2. Two heavily and positively p^+ -doped bifurcate regions G4 extend in the projections G3, so as to improve the electrical contact with these projections. Although the projections G3 of the illustrated embodiment are shown to have uniform thickness, it will be understood that they may have some other form and may, for instance, be Y-shaped as illustrated by the chain line L1 in the Figure.

The electrical field and the depletion regions in the component region 24 will be described briefly with reference to Figure 7 and Figure 8. These Figures illustrates parts of Figure 5 and 6 in larger scale. The region DP2, which is a depletion region, is shown adjacent the PN-junction 29 beneath the base region B3. A corresponding depletion region DP1 of the transistor BIP1 has been described in closer detail with reference to Figures 1 and 2. The field effect transistor JFET2 has a depletion region DP3 which extends between the projections G3, as shown by a broken defining line. The defining line of the region DP3 can be displaced by appropriate selection of the voltages applied to the connections 26 of the transistor JFET2. At the line A-A, this displacement takes place in a direction indicated by a double-headed arrow P0. The depletion region DP3 extends partly into the projections G3, as shown in the Figure at the ends of the projections. It should be noted that both gate projections G3 of the field effect transistor JFET2 extend from the surface of the component region 24 downwardly into said region. Similarly, the depletion region DP3 extends downwardly from

the surface of the component region. The electrical field strength in the component region is described by a curve C2. A digital value $1 \cdot 10^5$ denotes the electrical field strength along the curve in volt/cm that applies to the blocking state of the transistor device when the emitter E2 and the base connection B2 are earthed and the drain connection D2 is connected to a voltage of +100 V. The electrical field strength can be illustrated more accurately with a curve family similar to that illustrated in Figure 2, although only the curve C2 has been shown in order not to complicate the Figure unnecessarily. It will be seen from Figure 7 that the field strength is low, both in the depletion region DP2 beneath the transistor BIP2 and between the projections G3. The curve C2 in Figure 8 discloses the electrical field strength on the surface of the component region 24. The illustrated curve C2 is based on appraisals of the field strength, since it is difficult to take reliable measurements and because a reliable arithmetical model is at present lacking for the embodiment illustrated in Figure 5-8.

The relatively high field strength $2.5 \cdot 10^5$ V/cm at the edge of the base region B in Figure 2 is avoided in the inventive embodiment illustrated in Figures 5 and 6. This means that the series-connected transistors BIP2 and JFET2 provide a component which is able to withstand very high voltages. The alternative embodiment which includes the Y-shaped projections G3 in Figure 6 improves voltage durability still further, because the ends of these projections can be readily depleted of charge carriers. The series resistance of the transistor device between the source region S2 and the drain connection D2 can be kept low, because the distance between the projections G3 widens successively towards the drain connection.

Certain data related to the transistor device BIP1 and JFET1 illustrated in Figures 1 and 2 will be explained in more

detail with reference to Figures 9 and 10 and comparisons with known transistors will also be made. Figure 9 is a diagram in which the drain voltage V_D in volts is given on the abscissa and a normalized value of the current I expressed in mA is given on the ordinate. A full line curve 4μ discloses the characteristics of the transistor device shown in the Figures, this transistor device being formed in the monocrystalline wafer 3 of thickness $A1 = 4 \mu\text{m}$. Broken line curves 4.5μ and 5μ illustrate characteristics of transistor devices formed in monocrystalline wafers of thicknesses 4.5 and $5 \mu\text{m}$ respectively. A broken line curve μ illustrates a characteristic which is ideal from a signal processing aspect. It will be noted that the thinner the monocrystalline wafer 3, the closer the characteristics of the transistor device approach the desired ideal curve μ .

Figure 10 is a diagram in which the voltage V_B in volts is given on the abscissa and a normalized current value in ampere is given on the ordinate. A full line curve IC shows how the aforesaid current I varies with the voltage V_B at a drain voltage V_D of 7.5 volts. It will be noted that the current curve for a corresponding transistor of earlier known construction is in such good accord with the current curve of the inventive transistor that the two curves can hardly be distinguished from one another in the diagram. A difference which results in the inventive transistor producing a slightly lower current will only occur when voltages V_B lie beneath 0.20 volt. A full line curve IB1 illustrates a base current for the inventive transistor BIP1 and a broken line curve IB0 illustrates the base current for the known transistor just mentioned.

As before mentioned, the inventive transistor BIP1 is formed in the wafer 3 of thickness $A1 = 4 \mu\text{m}$, which shall be compared with the aforesaid known transistor which is formed in a monocrystalline wafer of thickness $25 \mu\text{m}$. The known transistor

has a heavily doped layer beneath its base region and the distance between this wafer and the base region of the transistor must be sufficiently large in order to prevent current breakthrough. Consequently, the relatively large thickness of the monocrystalline layer is a necessity, although it represents a serious drawback. In the case of present techniques, it is not possible to produce dielectrically isolating separation layers corresponding to the layer 5 in excessively thick mono-crystalline layers. The known transistor is therefore delimited by separation layers comprised of deep and heavily doped diffusions, which are space-demanding. This means that the known transistor will take up large surface areas on its monocrystalline layer.

The manner in which the aforesaid components are produced will now be described briefly with reference to Figures 11-14. The starting material is a so-called bonded wafer, comprising the silicon substrate 1, the isolating oxide layer 2 and the monocrystalline silicon wafer 3, as illustrated in Figure 11. Such a bonded wafer may be produced, for instance, in the manner described in the aforesaid European Patent Application No. A1-0,418,737 and is available commercially. The upper surface of the wafer 3 is coated with a photoresist layer 31, which is exposed in a predetermined pattern and developed to produce openings 32 in the layer 31. Deep trenches 33 are plasma etched through these openings, down to the isolating layer 2, and the photoresist layer 31 is removed. The sides of the trenches are oxidized to form silicon dioxide layers 34, and the remainders of the trenches 33 are filled with polycrystalline silicon 35, as shown in Figure 12. The component region 4 is delimited in this way. The wafer 3 is coated with a new photoresist mask 36 having an opening 37. Doping with positive doping material is effected through this opening, so as to obtain the base region B according to Figure 13. The mask 36 is removed and a further photoresist mask 38 is applied, this mask having openings 39

for negative doping of the emitter E1 and the drain connection D1. The mask 38 is removed and a new photoresist mask is applied and the base connection B1 is heavily and positively doped through the mask. This stage of manufacture has not been
5 shown in the Figure. This latter photoresist mask is removed and the surface of the wafer 3 is oxidized to form the isolating silicon dioxide layer 6, as illustrated in Figure 14. This layer 6 is coated with a mask 40 having openings 41 through which the connection openings 7 are etched in the
10 layer 6. The mask 40 is removed and the component is provided with external connections and protective layers, not shown in the drawings.

In the foregoing, the bipolar transistor BIP1 has been described connected in series with the field effect transistor
15 JFET1, and a method of producing these transistors. The base region B3 of the transistors BIP2 and JFET2 and the projections G3 of said base region can be produced simply by changing the configuration of the opening 37 in the mask 36. The illustrated bipolar transistors BIP1 and BIP2 are NPN
20 transistors, although it will be understood that the scope of the invention also embraces PNP transistors.

It was mentioned in the introduction that large field strengths may also occur in components intended for calculating or computing circuits that are connected to voltages
25 in the order of 3 to 5 volts. These components are extremely rapid and contain high concentrations of doping substances and are small in size. For instance, these components have a thickness, corresponding to the distance A1 in Figure 1, in the order of only about 0.5 μm . The invention can also be ap-
30 plied to these components, which have a high connecting voltage in relation to their size. It can be mentioned that in the case of these thin components, the aforesaid separation layer 5 can be replaced by a layer produced by so-called local

oxidization (LOCOS), which is a relatively simple isolation procedure.

Although the invention has been exemplified with silicon components, it will be understood that other semiconductor materials, such as germanium or gallium arsenide, may be used equally as well.

The inventive components provide several advantages in addition to their voltage durability. By applying the resurf technique in the aforescribed manner, the applied voltage is distributed over a large part of the component. Consequently, the component need only occupy a relatively small surface area of the substrate, as described above. In addition, the components may advantageously be made thin, which enables the components to be isolated laterally with the illustrated dielectrical separation layers 5 and 25 respectively. This results in a further reduction in the space required on the substrate. When practicing the invention, the requisite surface area of a semiconductor substrate which is to carry a specific number of components can be at least halved in comparison with earlier known techniques. This is particularly beneficial in the case of, for instance, subscriber line circuits in a telephone system in which each subscriber has its own line circuit. Another advantage afforded by the invention is that the components can be produced easily, since they are formed in a finished monocrystalline semiconductor layer and since their form is determined by selection of photoresist masks.



CLAIMS

- 1 A semiconductor device in a thin active layer with high breakdown voltage, said device having charge carrier depleted regions (DP1; DP2, DP3) of reduced electrical field strength
- 5 (E_D) and comprising
- a semiconductor body (1, 2, 4a; 21, 22, 24a, 24b)
 - a component region (4; 24) of semiconductor material carried by the semiconductor body and having an upper surface, which region is weakly doped with a first type (n) of doping
 - 10 material;
 - a dielectric isolating layer (2; 22) which delimits a lower surface of the component region (4; 24) from the semiconductor body;
 - an electrically delimiting separation layer (5; 10; 25)
 - 15 which extends along the remaining surfaces of the component region (4; 24) that border on the semiconductor body (1, 2, 4a; 21, 22, 24a, 24b);
 - a sunken region (B; B3, G3) in the component region (4; 24) that has a relatively low concentration of a second type (p)
 - 20 of doping material which is opposite to the first type of doping material, wherein the sunken region extends from the upper surface of the component region;
 - a PN-junction (9; 29) at the surface of the sunken region that delimits said region from a remaining part of the
 - 25 component region;
 - at least one semiconductor component (BIP1, JFET1; BIP2; JFET2) in the component region (4; 24); and
 - at least two electrical connections (8; 26) in the component region (4; 24), wherein the regions of reduced electrical
 - 30 field strength (DP1; DP2, DP3) are depleted of charge carriers by electrical voltages (V_E , V_B , V_D) applied to the electrical connections (8; 26) and a first of the charge carrier depleted regions (DP1; DP2) extends from the PN-junction (9; 29) to the dielectric isolating layer (2; 22), at least beneath a
 - 35 part of the sunken region (B; B3, G3).



c h a r a c t e r i z e d in that

- the semiconductor components include a bipolar transistor (BIP1; BIP2) which is connected in series to a second semiconductor component (JFET1; JFET2);
- 5 - in that the sunken region includes a base region (B; B3) of the bipolar transistor (BIP1; BIP2);
- in that the base region (B; B3) surrounds an emitter region (E1; E2) which is heavily doped (n^+) with the first type of doping material and is connected to one of the electrical
- 10 connections (8; 26);
- in that the base region (B; B3) has a base connection region (B1; B2) which is heavily doped (p^+) with the second type of doping material and which is connected to another of the electrical connections
- 15 (8; 26);
- in that the base connection region (B1; B2) includes a connection region (G1; G2) for the second, series-connected component (JFET1; JFET2); and
- in that the second semiconductor component (JFET1; JFET2)
- 20 has a heavily doped (n^+) connection region (D1; D2) in the said remaining part of the component region (4; 24) with a third of the electrical connections (8; 26),
- such that the electrical field strength (E_D) in the first depleted region (DIP1; DP2) lies beneath a breakdown field
- 25 strength (E_{CR}) for the semiconductor material.

2. A semiconductor device according to Claim 1, c h a r a c t e r i z e d in that the second semiconductor component (JFET1; JFET2) is a field effect transistor, wherein the connection region (D1; D2) of said transistor is doped with

30 doping material of said first type (n).

3. A semiconductor device according to Claim 1 or 2, in which the separation layer (25) has two mutually opposing dielectrically isolating walls on opposite sides of the component region (24), c h a r a c t e r i z e d in that



- the sunken region has two projections (G3) which extend in the component region (24) along said mutually opposite walls of the dielectrically isolating separation layer (25), wherein a second of the charge-carrier depleted regions (DP3) extends between the projections (G3).

4. A semiconductor device according to Claim 3, characterized in that the ends of the projections (G3) proximal to the base region (B3) have a greater cross width than the other ends of said projections.