WHAT IS CLAIMED IS:

1. A memory device, comprising:

a page including a plurality of memory cells coupled to a word line;

a plurality of page buffers coupled to the plurality of memory cells through a plurality of bit lines, respectively and divided into a plurality of page buffer groups each including at least two page buffers among the plurality of page buffers; and

a program operation controller configured to control the plurality of page buffers to perform bit line precharge operations initiated at different time points for each page buffer group among the plurality of page buffer groups during a program operation on the page,

wherein the program operation controller increases intervals between the time points at which the bit line precharge operations are initiated by the plurality of page buffer groups at a first timing during the program operation and decreases the intervals between the time points at which the bit line precharge operations are initiated by the plurality of page buffer groups at a second timing during the program operation.

2. The memory device according to claim 1, wherein:

the program operation controller provides a plurality of page buffer control signals that are activated at different time points to each of the plurality of page buffer groups, and

the plurality of page buffer groups perform the bit line precharge operations in response to the plurality of page buffer control signals,

respectively.

3. The memory device according to claim 2, further comprising a peripheral circuit configured to perform the program operation,

wherein the peripheral circuit comprises the plurality of page buffer groups, and performs a program voltage apply operation on the plurality of memory cells to be programmed to any one of first to n-th program states and a program verify operation for at least one of the first to n-th program states, where n is a natural number.

4. The memory device according to claim 3, wherein:

the program operation controller determines the first timing and the second timing depending on a progress of the program operation.

5. The memory device according to claim 4, wherein the progress of the program operation corresponds to a highest program state for which the program verify operation has passed, among the first to n-th program states.

6. The memory device according to claim 5, wherein the program operation controller adjusts the intervals based on a result of a comparison between the highest program state and one or more reference states.

7. The memory device according to claim 6, wherein the first timing

corresponds to a time when the highest program state is equal to or higher than a first reference state, among the one or more reference states.

8. The memory device according to claim 7, wherein the second timing corresponds to a time when the highest program state is equal to or higher than a second reference state different from the first reference state, among the one or more reference states.

9. The memory device according to claim 4, wherein:

the peripheral circuit performs one or more program loops, each including the program voltage apply operation and the program verify operation, and

the progress of the program operation is determined based on a program loop count indicating a number of program loops that are performed during the program operation.

10. The memory device according to claim 9, wherein the program operation controller adjusts the intervals based on a result of a comparison between the program loop count and one or more reference values.

11. The memory device according to claim 10, wherein the first timing corresponds to a time when the program loop count is equal to or greater than a first reference value, among the one or more reference values.

12. The memory device according to claim 11, wherein the second timing corresponds to a time when the program loop count is equal to or greater than a second reference value different from the first reference value, among the one or more reference values.

13. The memory device according to claim 12, wherein the second reference value is greater than the first reference value.

14. The memory device according to claim 1, wherein a length of a shortest period, among periods during which the bit line precharge operations are performed, is fixed at a default value, and

wherein, the default value is a minimum time required to precharge a potential of a bit line to a set value.

15. A method of operating a memory device, the memory device performing a program operation on a plurality of memory cells coupled to a plurality of page buffers through a plurality of bit lines respectively which are divided into a plurality of page buffer groups, the method comprising:

determining intervals between time points at which precharging of the plurality of bit lines is initiated by the plurality of page buffer groups;

performing bit line precharge operations to precharge the plurality of bit lines coupled to the plurality of memory cells initiated at different time points for each page buffer group among the plurality of page buffer

groups; and

performing program voltage applying operations to apply a program voltage to a word line coupled to the plurality of memory cells after the bit line precharge operations,

wherein the intervals are increased at a first timing in the program operation and decreased at a second timing in the program operation, and

wherein each of the page buffer groups includes at least two page buffers among the plurality of page buffers.

16. The method according to claim 15, wherein the program operation comprises one or more program loops, and

each of the one or more program loops comprises the program voltage applying operation on the plurality of memory cells to be programmed to any one of first to n-th program states and a program verify operation for at least one of the first to n-th program states, where n is a natural number.

17. The method according to claim 16, wherein the first timing and second timing are determined depending on a progress of the program operation.

18. The method according to claim 17, wherein the progress of the program operation corresponds to a highest program state for which the program verify operation has passed, among the first to n-th program

states, where n is a natural number.

19. The method according to claim 18, wherein the intervals are increased or decreased based on a result of a comparison between the highest program state and one or more reference states.

20. The method according to claim 17, wherein the progress of the program operation is determined based on a program loop count indicating a number of program loops that are performed during the program operation.

21. The method according to claim 18, wherein the intervals are increased or decreased based on a result of a comparison between the program loop count and one or more reference values.

22. The method according to claim 15, wherein a length of a shortest period, among periods during which the bit line precharge operations are performed, is fixed at a default value.