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BUS CONTROL LOGIC FOR COMPUTER SYSTEM HAVING DUAL BUS ARCHITECTURE

Abstract

A computer system is provided, comprising system memory and a memory controller for controlling access to system memory by means of a memory bus, a central processing unit electrically connected with the memory controller for reading and writing data to the system memory over the memory bus, a bus interface unit electrically connected with the memory controller by means of a system bus, and an input/output device electrically connected to the bus interface unit by an input/output bus. The memory controller incorporates logic for arbitrating between the central processing unit and the input/output device to determine which of the central processing unit and the input/output device should be granted access to the system memory through said memory bus. The bus interface unit incorporates logic for overriding the memory controller logic, in response to a series of predetermined operating conditions, and grant exclusive access to system memory to the input/output device.

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