FIG. 1

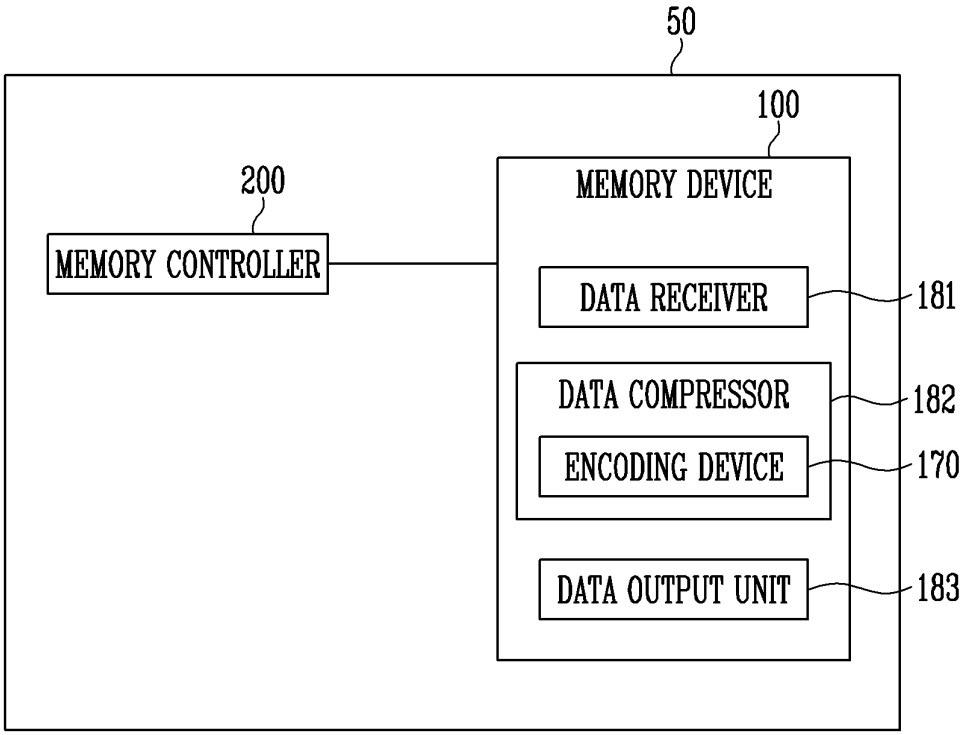

50
100
MEMORY DEVICE
200
MEMORY CONTROLLER
DATA RECEIVER
181
DATA COMPRESSOR
182
ENCODING DEVICE
170
DATA OUTPUT UNIT
183

FIG. 2

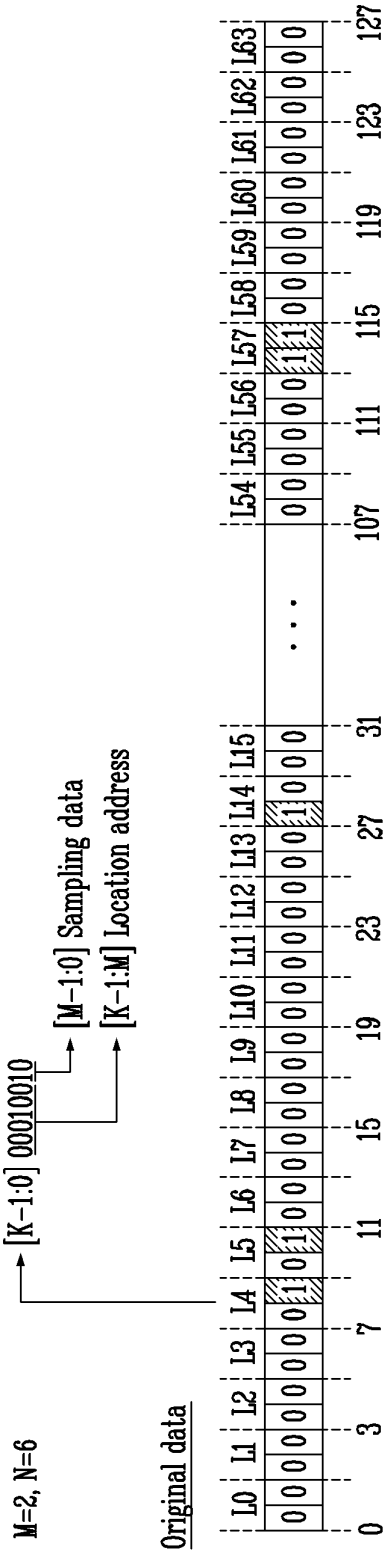

M=2, N=6
Original data
[K-1:0] 00010010
[M-1:0] Sampling data
[K-1:M] Location address
L0 L1 L2 L3 L4 L5 L6 L7 L8 L9 L10 L11 L12 L13 L14 L15 . . . L54 L55 L56 L57 L58 L59 L60 L61 L62 L63
0 3 7 11 15 19 23 27 31 107 111 115 119 123 127

FIG. 3

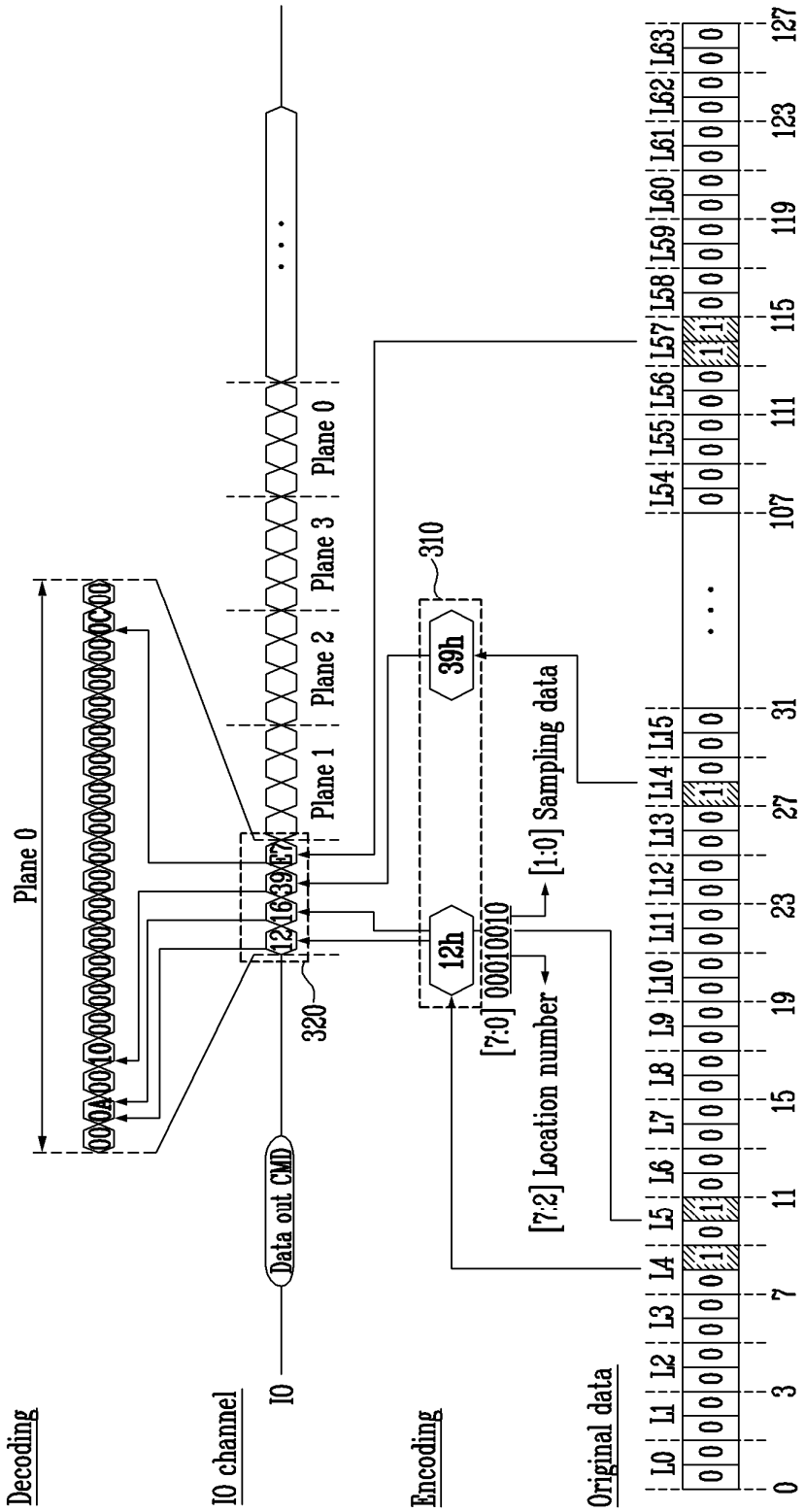

Decoding
IO channel
IO
Data out CMD
Plane 0
Plane 1
Plane 2
Plane 3
Plane 0
320
12h
39h
310
Encoding
[7:0] 00010010
[7:2] Location number
[1:0] Sampling data
Original data
L0 L1 L2 L3 L4 L5 L6 L7 L8 L9 L10 L11 L12 L13 L14 L15
L54 L55 L56 L57 L58 L59 L60 L61 L62 L63
0 3 7 11 15 19 23 27 31
107 111 115 119 123 127

FIG. 4

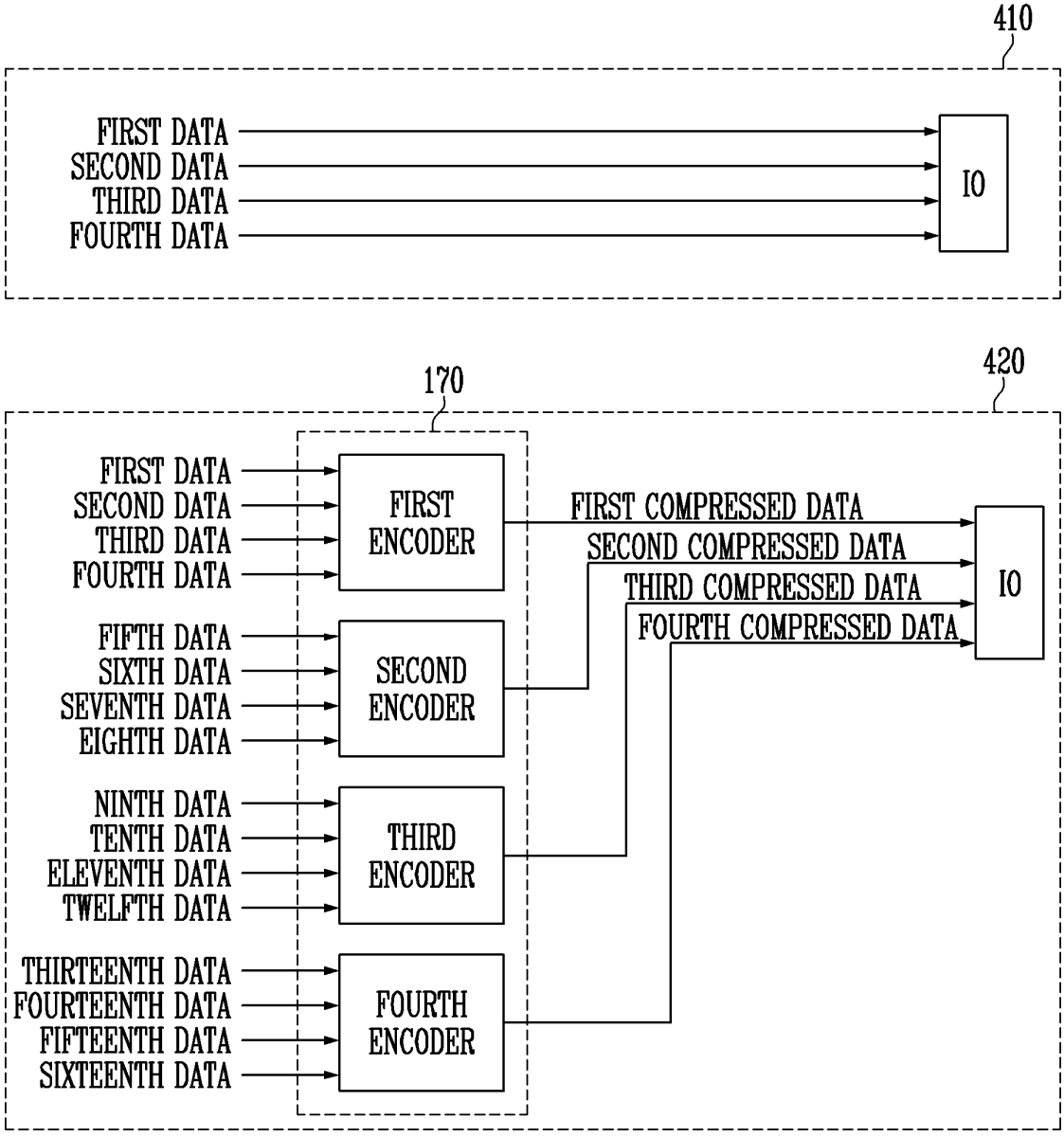

410
FIRST DATA
SECOND DATA
THIRD DATA
FOURTH DATA
IO
420
170
FIRST DATA
SECOND DATA
THIRD DATA
FOURTH DATA
FIRST ENCODER
FIFTH DATA
SIXTH DATA
SEVENTH DATA
EIGHTH DATA
SECOND ENCODER
NINTH DATA
TENTH DATA
ELEVENTH DATA
TWELFTH DATA
THIRD ENCODER
THIRTEENTH DATA
FOURTEENTH DATA
FIFTEENTH DATA
SIXTEENTH DATA
FOURTH ENCODER
FIRST COMPRESSED DATA
SECOND COMPRESSED DATA
THIRD COMPRESSED DATA
FOURTH COMPRESSED DATA
IO

FIG. 5

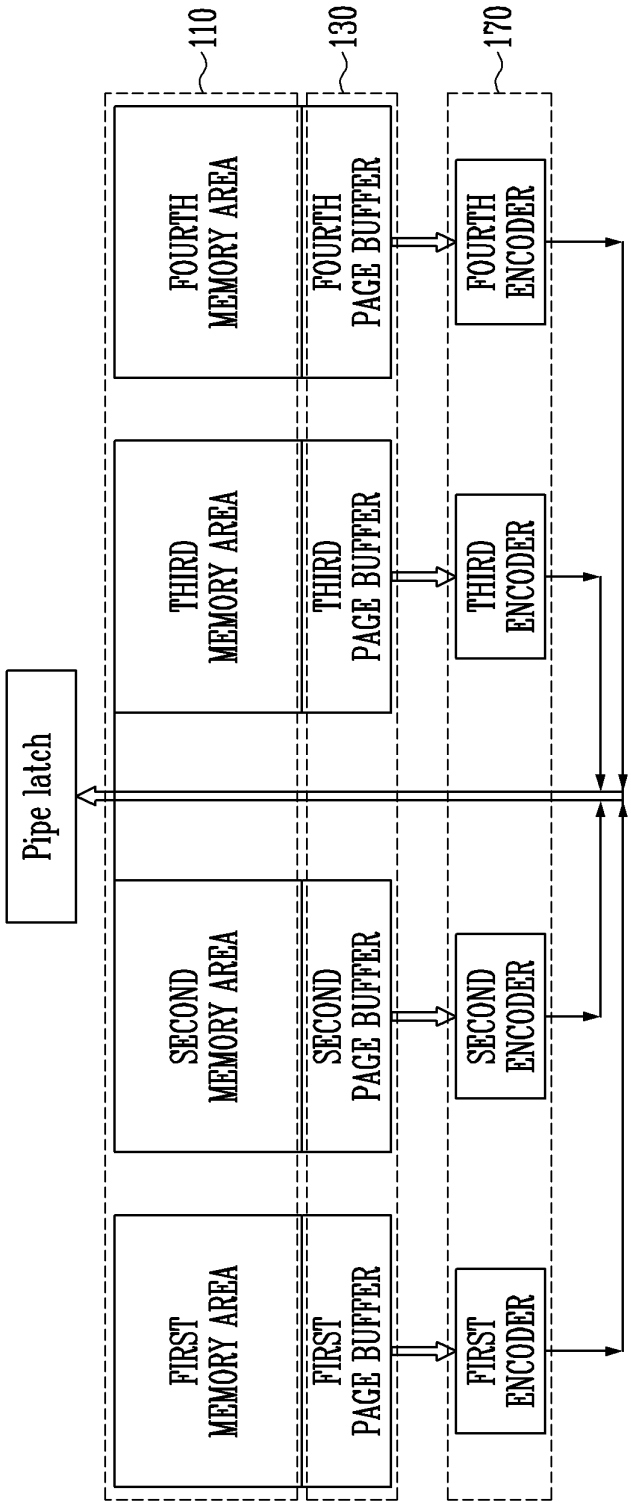

110
130
170
FOURTH MEMORY AREA
FOURTH PAGE BUFFER
FOURTH ENCODER
THIRD MEMORY AREA
THIRD PAGE BUFFER
THIRD ENCODER
Pipe latch
SECOND MEMORY AREA
SECOND PAGE BUFFER
SECOND ENCODER
FIRST MEMORY AREA
FIRST PAGE BUFFER
FIRST ENCODER

FIG. 6

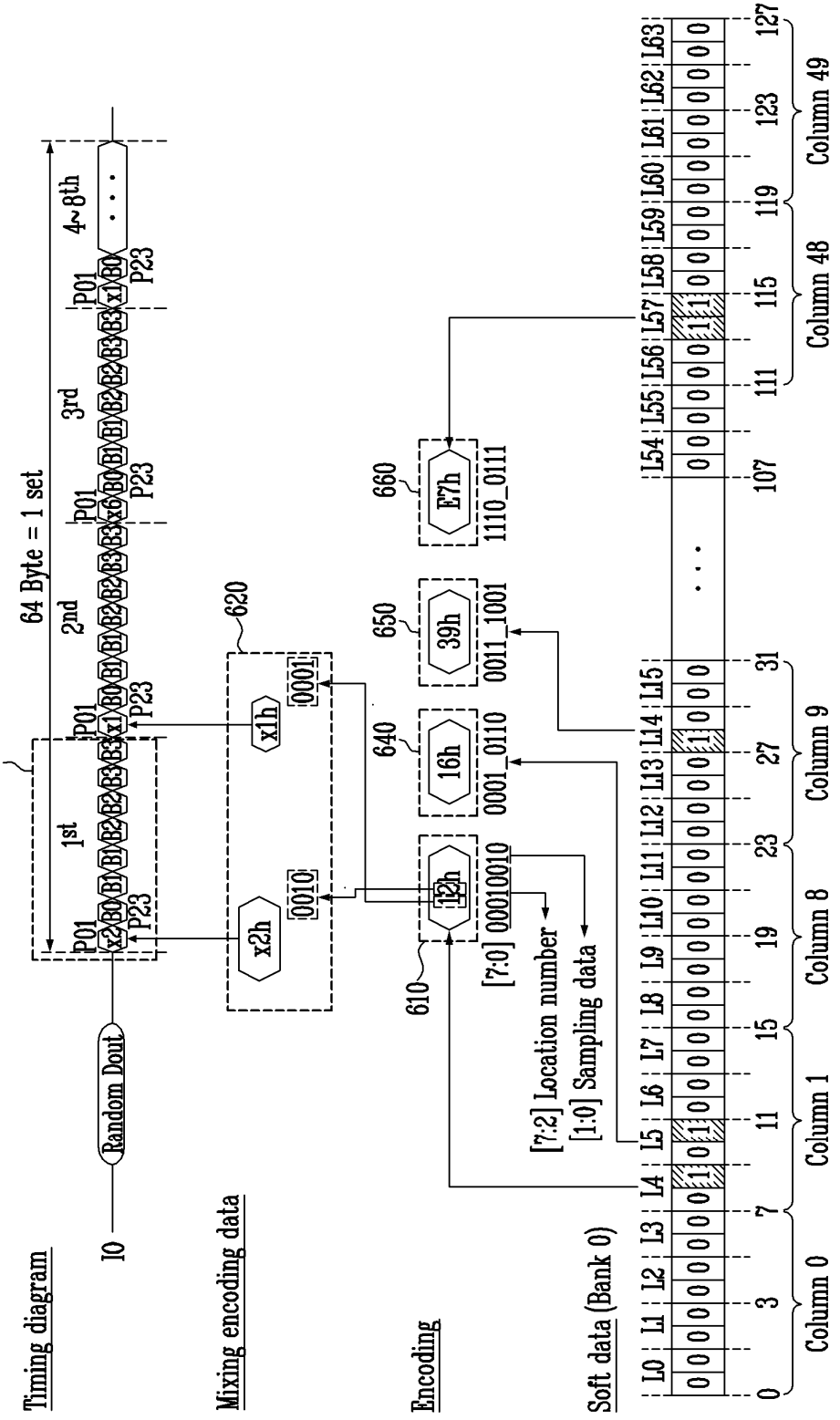

Timing diagram
IO
Random Dout
64 Byte = 1 set
1st
2nd
3rd
4~8th
630
Mixing encoding data
620
x2h
0010
x1h
0001
Encoding
610
640
16h
0001_0110
650
39h
0011_1001
660
E7h
1110_0111
[7:0] 00010010
[7:2] Location number
[1:0] Sampling data
Soft data (Bank 0)
Column 0
Column 1
Column 8
Column 9
Column 48
Column 49

FIG. 7

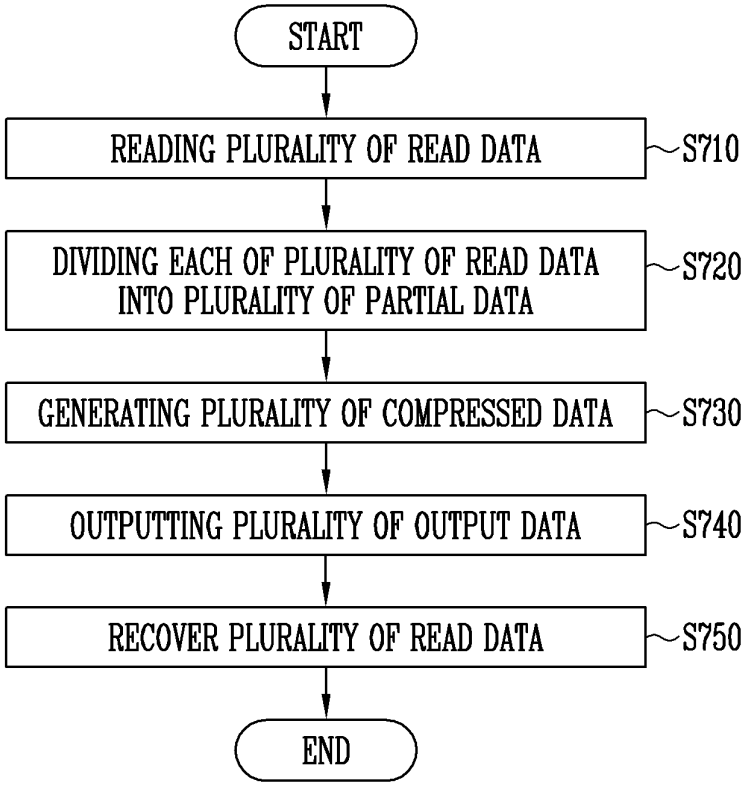

START
READING PLURALITY OF READ DATA
S710
DIVIDING EACH OF PLURALITY OF READ DATA INTO PLURALITY OF PARTIAL DATA
S720
GENERATING PLURALITY OF COMPRESSED DATA
S730
OUTPUTTING PLURALITY OF OUTPUT DATA
S740
RECOVER PLURALITY OF READ DATA
S750
END

FIG. 8

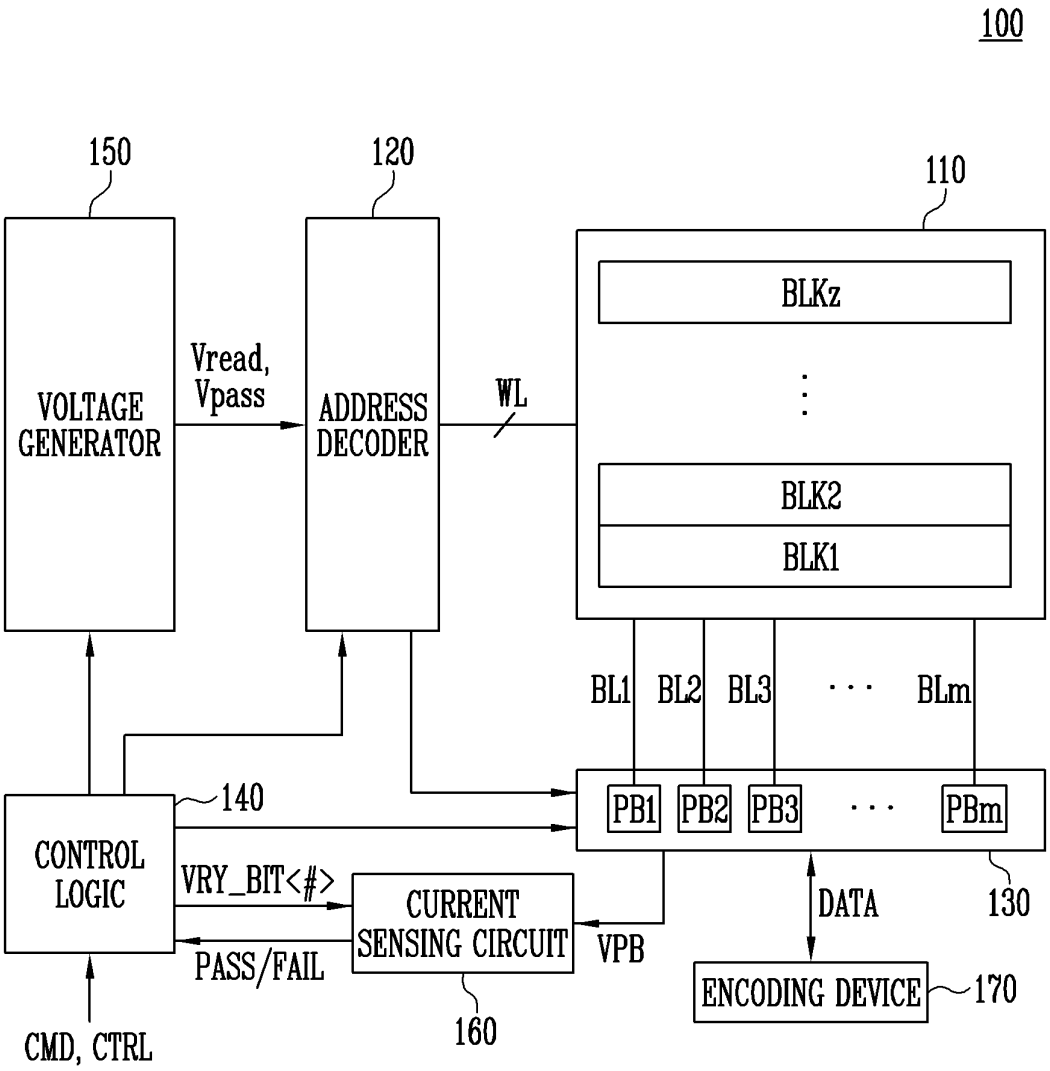

100
150
120
110
VOLTAGE GENERATOR
Vread, Vpass
ADDRESS DECODER
WL
BLKz
BLK2
BLK1
BL1
BL2
BL3
BLm
PB1
PB2
PB3
PBm
130
140
CONTROL LOGIC
VRY_BIT<#>
PASS/FAIL
CURRENT SENSING CIRCUIT
160
VPB
DATA
ENCODING DEVICE
170
CMD, CTRL

FIG. 9

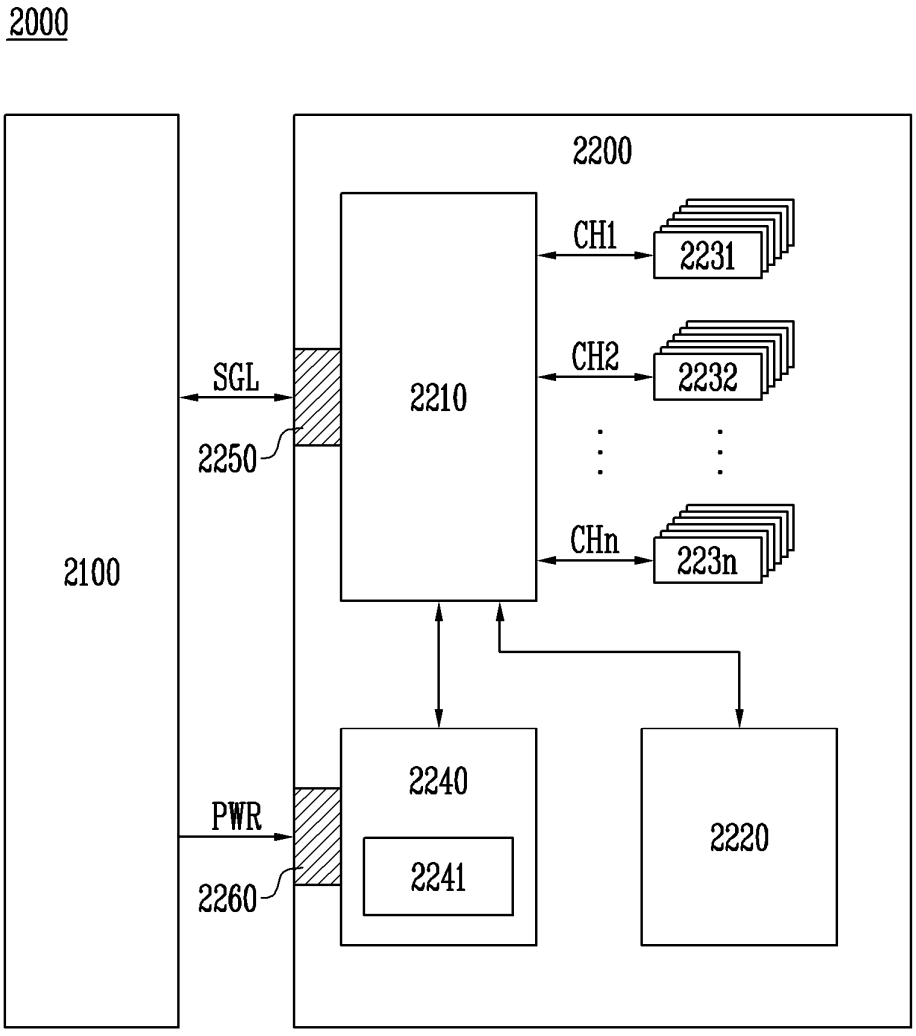

2000
2200
2100
2210
CH1
2231
CH2
2232
CHn
223n
SGL
2250
PWR
2260
2240
2241
2220

FIG. 10

