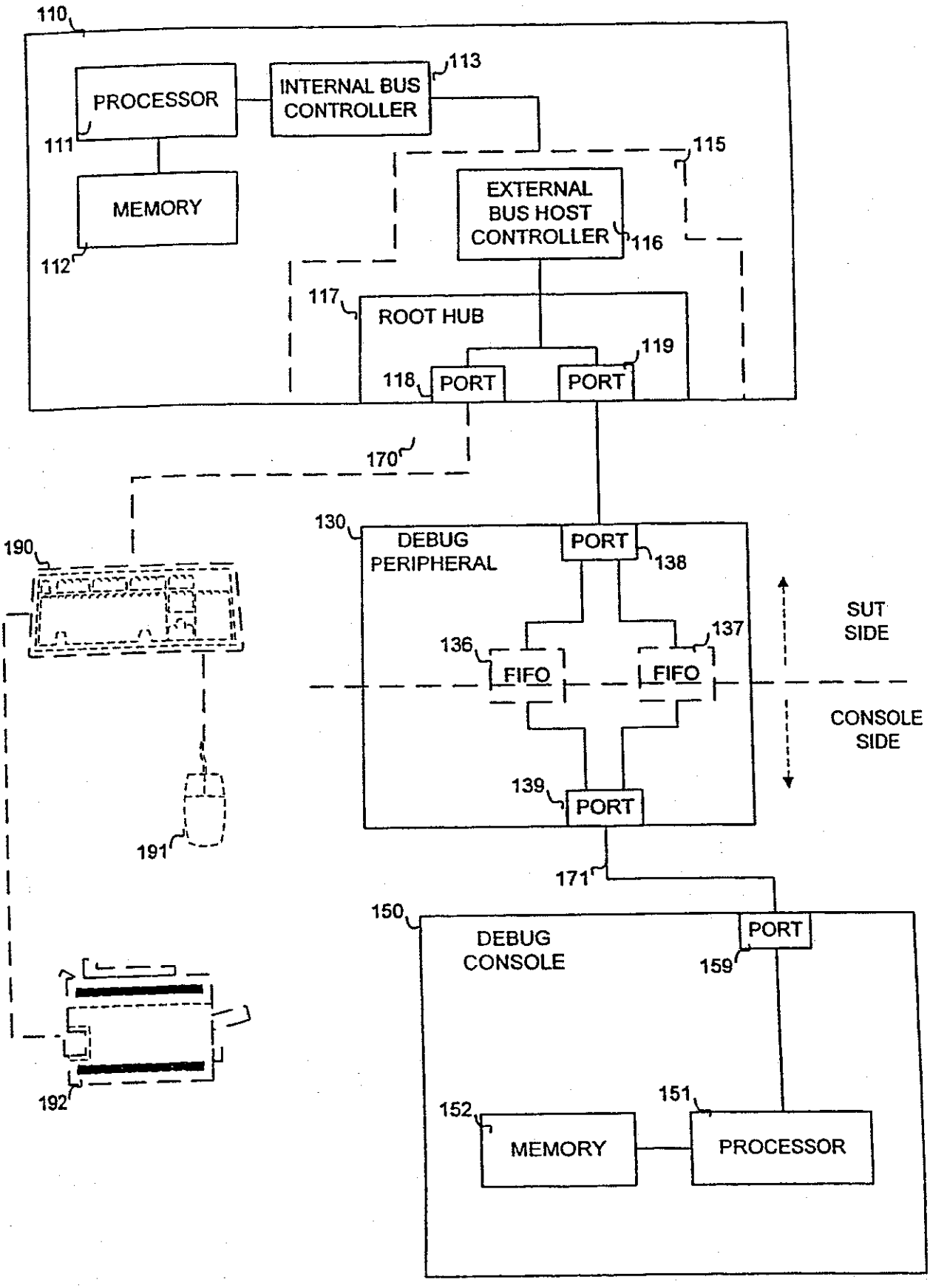

110
PROCESSOR
111
INTERNAL BUS CONTROLLER
113
MEMORY
112
115
EXTERNAL BUS HOST CONTROLLER
116
117
ROOT HUB
118
PORT
PORT
119
170
130
DEBUG PERIPHERAL
PORT
138
190
136
FIFO
FIFO
137
SUT SIDE
CONSOLE SIDE
139
PORT
191
171
150
DEBUG CONSOLE
PORT
159
151
152
MEMORY
PROCESSOR
192

FIG. 1

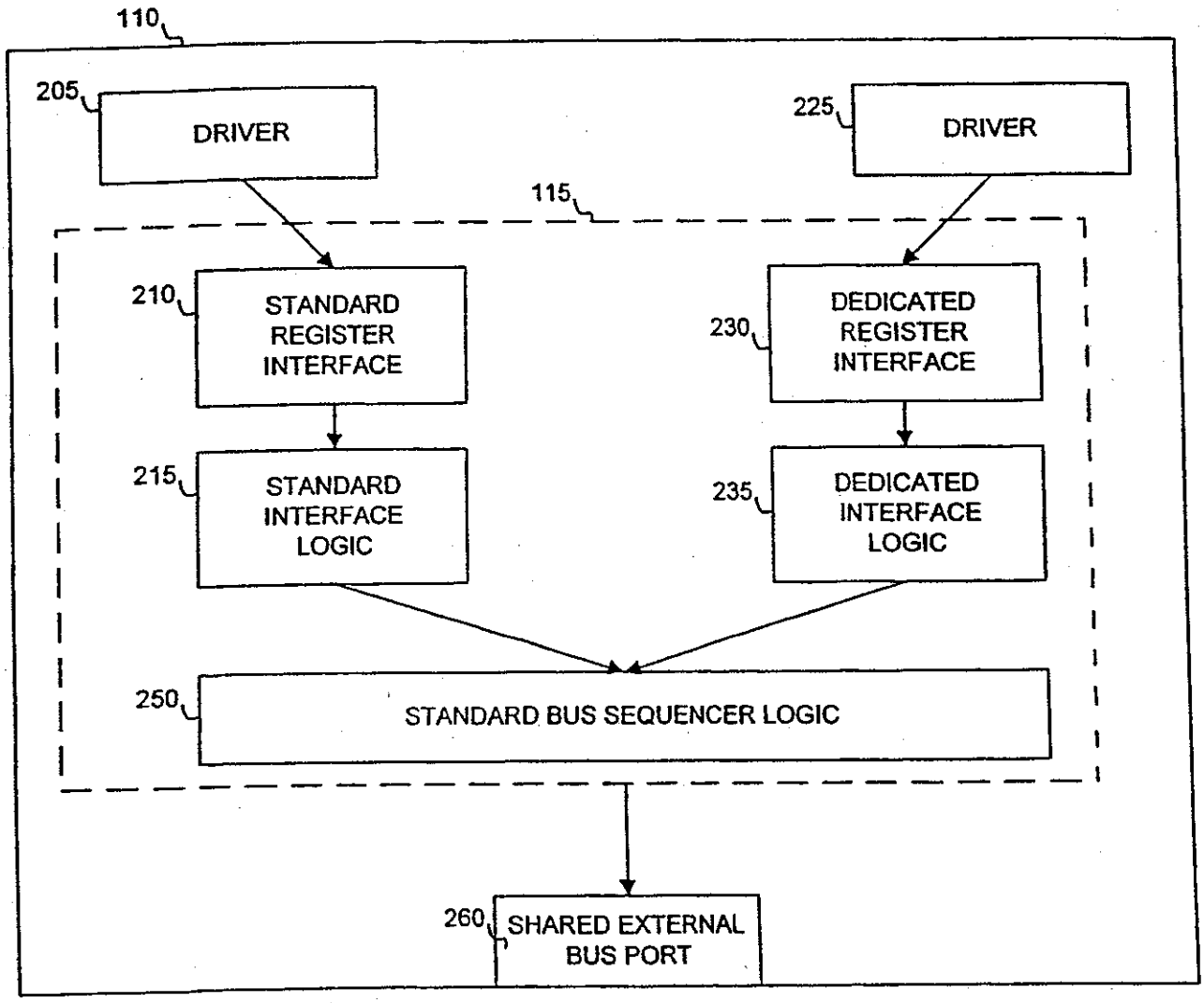

110
205
DRIVER
225
DRIVER
115
210
STANDARD REGISTER INTERFACE
230
DEDICATED REGISTER INTERFACE
215
STANDARD INTERFACE LOGIC
235
DEDICATED INTERFACE LOGIC
250
STANDARD BUS SEQUENCER LOGIC
260
SHARED EXTERNAL BUS PORT

FIG. 2