What is claimed is:

1. A method comprising:

forming a channel in a first type semiconductor portion to form a "U" shaped portion;

forming a dielectric material within the channel;

forming a control line over the dielectric material;

implanting a second type dopant into both top portions of the "U" shaped portion to form a pair of implanted regions; and

forming an upper first type semiconductor portion over one of the implanted regions.

2. The method of claim 1, wherein the first type semiconductor portion is P-doped and the second type dopant is an N-type dopant.

3. The method of claim 2, wherein implanting a second type dopant into both top portions of the "U" shaped portion includes heavily doping (N+) into at least one top portion of the "U" shaped portion.

4. The method of claim 3, wherein forming an upper first type semiconductor portion over one of the implanted regions includes forming a heavily doped (P+) portion over one of the implanted regions.

5. The method of claim 1, further including forming a first transmission line coupled to the other of the pair of implanted regions.

6. The method of claim 4, further including forming a second transmission line coupled to the upper first type semiconductor portion.

7. The method of claim 6, wherein the first and second transmission lines are formed substantially orthogonal.

8. The method of claim 6, wherein forming a second transmission line includes forming a first type semiconductor material and forming a metal cap material over the first type semiconductor material.

9. The method of claim 8, wherein forming the first type semiconductor material includes forming a heavily doped (P+) material.

10. A method comprising:

forming a conductor region beneath a first type semiconductor portion separated therefrom by a dielectric material;

forming a channel in the first type semiconductor portion to form a "U" shaped portion;

forming a dielectric material within the channel;

forming a control line over the dielectric material;

implanting a second type dopant into both top portions of the "U" shaped portion to form a pair implanted regions; and

forming an upper first type semiconductor portion over one of the implanted regions.

11. The method of claim 10, wherein forming a conductor region includes forming a metal region.

12. The method of claim 10, wherein forming the conductor region beneath the first type semiconductor portion separated therefrom by a dielectric material includes:

forming a dielectric material over a first type semiconductor substrate;

forming a conductor region over the dielectric material; and

flipping and bonding the conductor region to a second substrate

13. The method of claim 12, wherein forming the conductor region beneath the first type semiconductor portion further includes thinning the flipped first type semiconductor substrate using an implanted marker.

14. The method of claim 12, wherein flipping and bonding the conductor region to a second substrate includes flipping and bonding the conductor region to an oxidized surface material of a silicon substrate.

15. The method of claim 12, wherein flipping and bonding the conductor region to a second substrate includes forming an amorphous silicon material over the conductor region, and flipping and bonding the amorphous silicon material to an oxidized surface material of a silicon substrate.

16. A method comprising:

forming two vertically coupled P-N junctions on a first substrate;

forming a conductor region over the two vertically coupled P-N junctions;

flipping the first substrate, and bonding the conductor region to a dielectric material of a second substrate;

forming a third vertically coupled P-N junction on a back side of a portion of the first substrate;

forming a control line between two of the vertically coupled P-N junctions;

forming a buried transmission line from a portion of the conductor region; and

forming a second transmission line on top of the third vertically coupled P-N junction.

17. The method of claim 16, wherein forming two vertically coupled P-N junctions on a first substrate includes forming on a P-doped silicon substrate.

18. The method of claim 16, wherein forming a conductor region over the two vertically coupled P-N junctions includes forming a titanium conductor region.

19. The method of claim 16, wherein forming a conductor region over the two vertically coupled P-N junctions includes forming a tungsten conductor region.

20. The method of claim 16, further including forming an amorphous silicon material over the conductor region prior to flipping the first substrate, and bonding the conductor region to the dielectric material of the second substrate.

21. A method comprising:

forming a vertical stack of alternating conductivity type semiconductor material, including:

forming two vertically coupled P-N junctions on a first substrate;

forming a conductor region over the two vertically coupled P-N junctions;

flipping the first substrate, and bonding the conductor region to a dielectric material of a second substrate;

forming a third vertically coupled P-N junction on a back side of a portion of the first substrate;

forming trenches in the vertical stack to form an array of vertical pillars of alternating conductivity type semiconductor material; and

forming at least one control line in a trench between two adjacent pillars separated from a channel region by a dielectric material.

22. The method of claim 21, wherein forming at least one control line in the trench includes forming a single control line to operate a pair of adjacent channel regions on adjacent pillars in the array at the same time.

23. The method of claim 21, wherein forming at least one control line in the trench includes forming a pair of split control lines in the same trench to operate adjacent channel regions on adjacent pillars in the array separately.

24. The method of claim 21, wherein forming trenches includes forming trenches down to the conductor region.

25. The method of claim 21, further including etching a portion of the vertical stack underneath the at least one control line.

26. The method of claim 21, wherein forming two vertically coupled P-N junctions on a first substrate includes forming two vertically coupled P-N junctions on a P-type silicon substrate.

27. The method of claim 21, wherein bonding the conductor region to the dielectric material of the second substrate includes bonding the conductor region to a silicon oxide material on a silicon substrate.

28. The method of claim 21, further including forming a buried transmission line from a portion of the conductor region.

29. The method of claim 28, further including forming a second transmission line on top of the vertical pillars.

30. A semiconductor memory device, comprising:

an array of memory cells, each memory cell including a folded first conductivity type semiconductor region, each folded region having two upward facing ends;

a pair of second conductivity type semiconductor regions coupled to the upward facing ends;

a control line within the folded region between the two upward facing ends;

a first conductivity type semiconductor cap on one of the second conductivity type semiconductor regions; and

a first transmission line coupled to the other second conductivity type semiconductor region.

31. The semiconductor memory device of claim 30, wherein the first conductivity type is P-type and the second conductivity type is N-type.

32. The semiconductor memory device of claim 30, further including a second transmission line coupled to the semiconductor cap.

33. The semiconductor memory device of claim 32, wherein the second transmission line is substantially orthogonal to the first transmission line

34. The semiconductor memory device of claim 32, wherein the second transmission line includes a first conductivity type semiconductor material and a metal region.

35. The semiconductor memory device of claim 30, wherein the first transmission line is shared between two adjacent memory cells in the array.

36. The semiconductor memory device of claim 30, wherein the first transmission lines extend outwards to both sides of the array in an interleaved arrangement.

37. The semiconductor memory device of claim 35, wherein the first transmission lines extend outwards to both sides of the array in an interleaved arrangement.

What is claimed is:

1. An invention not claimed in any divisional application.