ABSTRACT OF THE DISCLOSURE

SCHEME FOR PLANARIZING THROUGH-SILICON VIAS

Generally, the subject matter disclosed herein relates to conductive via elements, such as through-silicon vias (TSV's), and methods for forming the same. One illustrative method disclosed herein includes forming a layer of isolation material above a via opening formed in a semiconductor device, the via opening extending into a substrate of the semiconductor device. The method also includes performing a first planarization process to remove at least an upper portion of the layer of isolation material formed outside of the via opening, and forming a conductive via element inside of the via opening after performing the first planarization process.

Fig. 2g