WHAT IS CLAIMED IS:

1. A package substrate in which a device chip mounted in a frame is covered by a mold resin, the package substrate comprising:

a metallic lead frame that includes first frame portions in a lattice shape along planned dividing lines demarcating a supporting portion on which the device chip is disposed and a plurality of first electrode portions extending linearly from each of the first frame portions on both sides in a first width direction of each of the first frame portions;

a connection frame that includes second frame portions in a lattice shape along the planned dividing lines and a plurality of second electrode portions extending linearly from each of the second frame portions on both sides in a second width direction of each of the second frame portions, the connection frame being superposed on a side of the lead frame on which the device chip is disposed; and

the mold resin that covers the connection frame and the device chip disposed to be electrically connected to the first electrode portions of the lead frame, wherein

distal ends of the second electrode portions are formed in a shape protruding to the first electrode

portions more than the second frame portions and are connected to the first electrode portions of the lead frame, the second frame portions are superposed on the first frame portions at an interval from the first frame portions, and

the connection frame forms an electrode when electroplating processing is applied to sections of the first electrode portions, the sections being formed by severing the first electrode portions from the first frame portions.

2. A method for processing a package substrate in which a device chip mounted in a frame is covered by a mold resin,

the package substrate including

a metallic lead frame that includes first frame portions in a lattice shape along planned dividing lines demarcating a supporting portion on which the device chip is disposed and a plurality of first electrode portions extending linearly from each of the first frame portions on both sides in a first width direction of each of the first frame portions,

a connection frame that includes second frame portions in a lattice shape along the planned dividing lines and a plurality of second electrode

portions extending linearly from each of the second frame portions on both sides in a second width direction of each of the second frame portions, the connection frame being superposed on a side of the lead frame on which the device chip is disposed, and

the mold resin that covers the connection frame and the device chip disposed to be electrically connected to the first electrode portions of the lead frame, wherein distal ends of the second electrode portions are formed in a shape protruding to the first electrode portions more than the second frame portions and are connected to the first electrode portions of the lead frame, the second frame portions are superposed on the first frame portions at an interval from the first frame portions,

the method comprising:

a cut groove forming step of forming a cut groove having a depth not reaching the connection frame covered by the mold resin, by making a first cutting blade cut into one of the first frame portions of the lead frame along corresponding one of the planned dividing lines on a top surface on which the lead frame of the package substrate is exposed, and exposing, in the cut groove, cut surfaces of the first electrode portions that are

severed when the first frame portion is cut;

a plating processing step of, after the cut groove forming step is performed, covering the exposed cut surfaces of the first electrode portions with a plating layer by electroplating by applying a voltage to the severed first electrode portions via the connection frame;

a dividing step of, after the plating processing step is performed, dividing the package substrate into individual packaged chips by cutting a center of the cut groove by a second cutting blade thinner than the first cutting blade to severe the connection frame and the mold resin; and

a solder fixing step of connecting the first electrode portions of one of the packaged chips that have undergone plating processing and electrodes of a wiring board as a mounting destination to one another by solder, with the top surface of the packaged chip disposed to face the wiring board.

3. A packaged chip obtained by dividing a package substrate, in which a device chip mounted on a supporting portion of a metallic lead frame is covered by a mold resin,

the package substrate including

the metallic lead frame that includes first frame portions in a lattice shape along planned dividing lines demarcating the supporting portion on which the device chip is disposed and a plurality of first electrode portions extending linearly from each of the first frame portions on both sides in a first width direction of each of the first frame portions,

a connection frame that includes second frame portions in a lattice shape along the planned dividing lines and a plurality of second electrode portions extending linearly from each of the second frame portions on both sides in a second width direction of each of the second frame portions, the connection frame being superposed on a side of the lead frame on which the device chip is disposed, and

the mold resin that covers the connection frame and the device chip disposed to be electrically connected to the first electrode portions of the lead frame, wherein distal ends of the second electrode portions are formed in a shape protruding to the first electrode portions more than the second frame portions and are connected to the first electrode portions of the lead frame, the second frame portions are superposed on the first frame portions at an interval from the first

frame portions,

wherein

a top surface of the packaged chip on which the supporting portion is exposed and a side surface of the packaged chip are connected to each other by a stepped portion having a predetermined height and width,

each of the first electrode portions of the lead frame electrically connected to the device chip is exposed on the top surface of the packaged chip and a surface of the stepped portion that is continuous with the top surface,

a section of each of the second electrode portions of the connection frame, each of the second electrode portions having an end portion connected to each of the first electrode portions, is exposed on a side surface continuous from the stepped portion to an undersurface of the packaged chip, and

each of the first electrode portions is covered by a plating layer, but each of the second electrode portions of the connection frame is not covered by the plating layer.

4. The package substrate according to claim 1, wherein the distal ends of the first electrode portions are connected to wires, and the first electrode portions

are thereby electrically connected to the device chips.

5. The package substrate according to claim 1, wherein the distal ends of the second electrode portions are arranged closer to the second frame portions than the distal ends of the first electrode portions.