SEMICONDUCTOR DEVICES

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This patent application claims the benefit of priority to Korean Patent Application No. 10-2023-0015676 filed on 6 February 2023 in the Korean Intellectual Property Office, the disclosure of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] Example embodiments of the present disclosure relate to semiconductor devices.

BACKGROUND

[0003] In answer to demands for high integration and miniaturization of a semiconductor device, a size of a semiconductor device has been miniaturized. Accordingly, a semiconductor device including a stacked transistor such as a complementary field effect transistor (CFET) stack has been introduced to reduce a corresponding area compared to an area of a corresponding non-stacked device.

SUMMARY

[0004] Some example embodiments of the present disclosure are to provide semiconductor devices having improved electrical properties and reliability.

[0005] According to some example embodiments of the present disclosure, a semiconductor device includes a lower structure; a barrier layer on the lower structure; and an upper structure on the barrier layer, wherein the lower structure includes lower source/drain regions spaced apart from each other in a first direction; lower active layers spaced apart from each other in a vertical direction, between the lower source/drain regions, and connected to the lower source/drain regions; and a lower gate structure extending in a second direction perpendicular to the first direction and including portions below each of the lower active layers, wherein the upper structure includes upper source/drain regions spaced apart from each other in a first

direction and vertically overlapping the lower source/drain regions; upper active layers spaced apart from each other in the vertical direction, between the upper source/drain regions, connected to the upper source/drain regions, and vertically overlapping the lower active layers; and an upper gate structure extending in the second direction, including portions on each of the upper active layers, and vertically overlapping the lower gate structure, and wherein the uppermost lower active layer of the lower active layers and the lowermost upper active layer of the upper active layers are in contact with the barrier layer.

[0006] According to some example embodiments of the present disclosure, a semiconductor device includes a first structure; a barrier layer on the first structure; and a second structure on the barrier layer, wherein the first structure includes first source/drain regions spaced apart from each other in a first direction; first channel layers spaced apart from each other in a vertical direction, between the first source/drain regions, and connected to the first source/drain regions; and a first gate structure extending in a second direction perpendicular to the first direction and including portions below the first channel layers, respectively, wherein the second structure includes second source/drain regions spaced apart from each other in the first direction; second channel layers spaced apart from each other in the vertical direction, between the second source/drain regions, and connected to the second source/drain regions; and a second gate structure extending in the second direction and including portions on the second channel layers, respectively, wherein the barrier layer includes a first portion between an uppermost first channel layer among the first channel layers and a lowermost second channel layer among the second channel layers, and a second portion extending from the first portion to a region between the first source/drain regions and the second source/drain regions, and wherein at least one of the upper surface and the lower surface of the second portion has a curved shape.

[0007] According to some example embodiments of the present disclosure, a semiconductor device includes lower channel layers and upper channel layers stacked in a vertical direction; lower source/drain regions spaced apart from each other on a first level; upper source/drain regions spaced apart from each other on a second level higher than the first level; lower

channel layers between the lower source/drain regions and spaced apart from each other in a vertical direction; upper channel layers between the upper source/drain regions and spaced apart from each other in the vertical direction; a barrier layer between an uppermost lower channel layer of the lower channel layers and a lowermost upper channel layer of the upper channel layers, and between the lower source/drain regions and the upper source/drain regions; a lower gate structure below the barrier layer and extending by covering an upper surface, a side surface, and a lower surface of at least one of the lower channel layers; an upper gate structure on the barrier layer and extending by covering an upper surface, a side surface, and a lower surface of at least one of the upper channel layers; a lower contact structure below the lower source/drain regions and electrically connected to the lower source/drain regions; and an upper contact structure on the upper source/drain regions and electrically connected to the upper source/drain regions.

BRIEF DESCRIPTION OF DRAWINGS

[0008] The above and other aspects, features, and advantages of the present disclosure will be more clearly understood from the following detailed description, taken in combination with the accompanying drawings, in which:

[0009] FIG. 1 is a plan diagram illustrating a semiconductor device according to some example embodiments of the present disclosure;

[0010] FIGS. 2A and 2B are cross-sectional diagrams illustrating a semiconductor device according to some example embodiments of the present disclosure;

[0011] FIGS. 3A and 3B are cross-sectional diagrams illustrating a semiconductor device according to some example embodiments of the present disclosure;

[0012] FIGS. 4, 5, 6, 7, 8A and 8B are cross-sectional diagrams illustrating a semiconductor device according to some example embodiments of the present disclosure; and

[0013] FIGS. 9A, 9B, 10A, 10B, 11, 12, 13, 14, 15A, 15B, 16A, 16B, 17A, 17B, 18A, 18B, 19A, 19B, 20A, 20B, 21A and 21B are cross-sectional diagrams illustrating processes of a method of manufacturing a semiconductor device in order according to some example

embodiments of the present disclosure.

DETAILED DESCRIPTION

[0014] Hereinafter, example embodiments of the present disclosure will be described as follows with reference to the accompanying drawings.

[0015] FIG. 1 is a plan diagram illustrating a semiconductor device according to some example embodiments.

[0016] FIGS. 2A and 2B are cross-sectional diagrams illustrating a semiconductor device in some example embodiments, taken along line I-I' and II-II' in FIG. 1. For ease of description, only a portion of components of a semiconductor device are illustrated in FIG. 1.

[0017] Referring to FIGS. 1 to 2B, a semiconductor device 100 may include a lower structure, a barrier layer 170 on the lower structure, and an upper structure on the barrier layer 170. The semiconductor device 100 further may include a contact structure 180, a gate contact structure 190, first to fifth interlayer insulating layers 191, 192, 193, 194, and 195, and first and second wirings M1 and M2.

[0018] In some example embodiments, the terms "first structure" and "second structure" may be referred to as "lower structure" and "upper structure," respectively, "first gate structure," "first channel layers," "first source/drain regions," and "first contact structure" may be referred to as "lower gate structure," "lower channel layers," "lower source/drain regions," and "lower contact structure," respectively, and "second gate structure" structure," "second channel layers," "second source/drain regions," and "second contact structure" may be referred to as "upper gate structure," "upper channel layers," "upper source/drain regions," and "upper contact structure", respectively.

[0019] The lower structure may include a substrate 101 including an active region 105 extending in the first direction X, a lower gate structure 160A intersecting the active region 105 and extending in the second direction Y on the substrate 101, lower channel layers 140A spaced apart from each other in the third direction Z perpendicular to an upper surface of the substrate 101 and surrounded by a lower gate structure 160A on the active region 105, and

lower source/drain regions 150A disposed on the active region 105 on at least one side of the lower gate structure 160A and connected to the lower channel layers 140A.

[0020] The upper structure may include an upper gate structure 160B disposed on the lower gate structure 160A and the barrier layer 170, intersecting the active region 105 on the substrate 101, and extending in the second direction Y, upper channel layers 140B spaced apart from each other in the third direction Z and disposed to be surrounded by an upper gate structure 160B on the active region 105, and upper source/drain regions 150B disposed on at least one side of the upper channel layers 140B on the active region 105 and the barrier layer 170 and connected to the upper channel layers 140B.

[0021] The substrate 101 may have an upper surface extending in X and Y-directions. The substrate 101 may include a semiconductor material, for example, a group IV semiconductor, a group III-V compound semiconductor, or a group II-VI compound semiconductor. For example, the group IV semiconductor may include silicon, germanium, or silicon-germanium. The substrate 101 may be provided as a bulk wafer, an epitaxial layer, a silicon on insulator (SOI) layer, or a semiconductor on insulator (SeOI) layer.

[0022] The device isolation layer 110 may define an active region 105 in the substrate 101. The device isolation layer 110 may be formed by, for example, a shallow trench isolation (STI) process. The device isolation layer 110 may expose an upper surface of the active region 105, or may partially expose an upper portion. In some example embodiments, the device isolation layer 110 may have a curved upper surface to have a higher level toward the active region 105. The device isolation layer 110 may be formed of an insulating material. The device isolation layer 110 may be, for example, oxide, nitride, or a combination thereof.

[0023] A channel structure 140 including lower channel layers 140A and upper channel layers 140B vertically spaced apart from each other on the active region 105, a gate structure 160 extending by intersecting the active region 105 and including a lower gate electrode 163A and an upper gate electrode 163B, source/drain regions 150 in contact with the channel structure 140, and a contact structure 180 connected to the source/drain regions 150 may be further included.

[0024] In the semiconductor device 100, the active region 105 may have a fin structure, and the lower gate electrode 163A and the upper gate electrode 163B may be disposed between the active region 105 and the channel structure 140, between the lower channel layers 140A and upper channel layers 140B of the channel structure 140, and on the channel structure 140. Accordingly, the semiconductor device 100 may include transistors having a multi bridge channel FET (MBCFET^{TM}) structure, which is a gate-all-around type field effect transistor. In some example embodiments, a semiconductor device may include transistors having a complementary FET (CFET) structure.

[0025] The gate structure 160 may include a lower gate structure 160A and an upper gate structure 160B.

[0026] The gate structure 160 may be disposed to intersect the active region 105 and channel structure 140 and to extend in a second direction, for example, in the Y-direction, on the active region 105 and the channel structure 140. Functional channel regions of the transistors may be formed in the active region 105 and/or the channel structure 140 intersecting the lower gate electrode 163A of the gate structure 160.

[0027] The lower gate structure 160A may include a lower gate electrode 163A, and a lower gate dielectric layer 162A disposed between the lower gate electrode 163A and the first to fourth lower channel layers 141A, 142A, 143A, and 144A. The lower gate structure 160A may extend in a second direction Y perpendicular to the first direction X, and may include portions disposed below each of the lower channel layers 140A. The lower gate structure 160A may surround a lower surface, an upper surface, and a side surface of each of the one or more lower channel layers 140A and the lowermost lower channel layer 141A in the second direction Y, and may cover the lower surface and side surface of the uppermost lower channel layer 144A.

[0028] The upper gate structure 160B may include an upper gate electrode 163B, an upper gate dielectric layer 162B between the upper gate electrode 163B and the first to fourth upper channel layers 141B, 142B, 143B, and 144B, gate spacers 164 on the side surfaces of the upper gate electrode 163B. The upper gate structure 160B may extend in the second direction

Y, may include portions disposed on the upper channel layers 140B, respectively, and may vertically overlap the lower gate structure 160A. The upper gate structure 160B may surround a lower surface, an upper surface and a side surface of each of the one or more upper channel layers 140B and the uppermost upper channel layer 144B in the second direction Y, and may cover an upper surface and side surface of the lowermost upper channel layer 141B.

[0029] The lower gate dielectric layer 162A may be disposed between the active region 105 and the lower gate electrode 163A and between the lower channel layers 140A and the lower gate electrode 163A, and may be disposed to cover at least a portion of the surfaces of the lower gate electrode 163A. For example, the lower gate dielectric layer 162A may be disposed to surround the entirety of surfaces other than the uppermost surface of the lower gate electrode 163A.

[0030] The upper gate dielectric layer 162B may be disposed between the upper channel layers 140B and the upper gate electrode 163B, and may be disposed to cover at least a portion of the surfaces of the upper gate electrode 163B. For example, the upper gate dielectric layer 162B may be disposed to surround the entirety of surfaces other than the uppermost surface of the upper gate electrode 163B. The upper gate dielectric layer 162B may extend to a region between the upper gate electrode 163B and the gate spacers 164, but some example embodiments thereof are not limited thereto.

[0031] The lower gate dielectric layer 162A and the upper gate dielectric layer 162B may include an oxide, a nitride, or a high-κ material. The high-κ material may refer to a dielectric material having a dielectric constant higher than that of silicon oxide (SiO_2). The high-κ material may be one of, for example, aluminum oxide (Al_2O_3), tantalum oxide (Ta_2O_3), titanium oxide (TiO_2), yttrium oxide (Y_2O_3), zirconium oxide (ZrO_2), zirconium silicon oxide ($ZrSi_xO_y$), hafnium oxide (HfO_2), hafnium silicon oxide ($HfSi_xO_y$), lanthanum oxide (La_2O_3), lanthanum aluminum oxide ($LaAl_xO_y$), lanthanum hafnium oxide ($LaHf_xO_y$), hafnium aluminum oxide ($HfAl_xO_y$), and/or praseodymium oxide (Pr_2O_3). In some example embodiments, the lower gate dielectric layer 162A and the upper gate dielectric layer 162B may include a multilayer film.

[0032] The lower gate electrode 163A may fill a region between the first to fourth lower channel layers 141A, 142A, 143A, and 144A on the active region 105 may extend to the lower channel layers 140A. The lower gate electrode 163A may be spaced apart from the first to fourth lower channel layers 141A, 142A, 143A, and 144A by the lower gate dielectric layers 162A.

[0033] The upper gate electrode 163B may fill a region between the first to fourth upper channel layers 141B, 142B, 143B, and 144B on the barrier layer 170 and may extend to the upper channel layers 140B. The upper gate electrode 163B may be spaced apart from the first to fourth upper channel layers 141B, 142B, 143B, and 144B by the upper gate dielectric layer 162B.

[0034] The lower gate electrode 163A and the upper gate electrode 163B may include a conductive material, for example, a metal nitride such as titanium nitride (TiN), tantalum nitride (TaN), or tungsten nitride (WN), and/or a metal material such as aluminum (Al), tungsten (W), or molybdenum (Mo) or semiconductor materials such as doped polysilicon. In some example embodiments, the lower gate electrode 163A and the upper gate electrode 163B may include two or more multilayers. In some example embodiments, the lower gate electrode 163A and the upper gate electrode 163B may be formed of a material having an appropriate work function in consideration of a desired threshold voltage. The lower gate electrode 163A may include an N-type work function layer, and the upper gate electrode 163B may include a P-type work function layer, but some example embodiments thereof are not limited thereto. In some example embodiments, the lower gate electrode 163A may include a P-type work function layer, and the upper gate electrode 163B may include an N-type work function layer.

[0035] The gate spacers 164 may be disposed on both side surfaces of the upper gate electrode 163B on the upper channel layers 140B. The gate spacers 164 may insulate the upper source/drain regions 150 from the upper gate electrode 163B. The gate spacers 164 may have a multilayer structure in some example embodiments. The gate spacers 164 may be formed of oxide, nitride, and oxynitride, and may be formed of a low-κ film, for example.

[0036] The channel structure 140 may include lower channel layers 140A and upper channel layers 140B. In some example embodiments, “lower active layers” and “upper active layers” in some example embodiments may be referred to as “lower channel layers” and “upper channel layers,” respectively.

[0037] The lower channel layers 140A may include first to fourth lower channel layers 141A, 142A, 143A, and 144A, which are two or more channel layers disposed in order and spaced apart from each other in a direction perpendicular to the upper surface of the substrate 101, for example, in the Z-direction, on the active region 105. The first to fourth lower channel layers 141A, 142A, 143A, and 144A may be disposed between the lower source/drain regions 150A, may be connected to the lower source/drain regions 150A, and may be spaced apart from the upper surface of the active region 105. The lower channel layers 140A may include a lowermost lower channel layer 141A, an uppermost lower channel layer 144A, and one or more lower channel layers 140A disposed between the lowermost lower channel layer 141A and the uppermost lower channel layer 144A.

[0038] The upper channel layers 140B may include two or more plurality of channel layers, first to fourth upper channel layers 141B, 142B, 143B, and 144B disposed in order and spaced apart from each other in a direction perpendicular to the upper surface of the barrier layer 170, for example, in the Z-direction, on the barrier layer 170. The upper channel layers 140B may include the lowermost upper channel layer 141B, an uppermost upper channel layer 144B, and one or more upper channel layers 140B disposed between the lowermost upper channel layer 141B and the uppermost upper channel layer 144B. The first to fourth upper channel layers 141B, 142B, 143B, and 144B may be connected to the upper source/drain regions 150B. The upper channel layers 140B may vertically overlap the lower channel layers 140A.

[0039] The first to fourth lower channel layers 141A, 142A, 143A, and 144A and the first to fourth upper channel layers 141B, 142B, 143B, and 144B may have the same width or similar widths as that of the active region 105 in the Y-direction and may have the same width or similar width as that of the gate structure 160 in the X-direction. However, in some example embodiments, the first to fourth lower channel layers 141A, 142A, 143A, and 144A and the

first to fourth upper channel layers 141B, 142B, 143B, and 144B may have a reduced width such that the side surfaces may be disposed below the gate structure 160 in the X-direction.

[0040] The first to fourth lower channel layers 141A, 142A, 143A, and 144A and the first to fourth upper channel layers 141B, 142B, 143B, and 144B may be formed of a semiconductor material, for example, silicon (Si), silicon germanium (SiGe), and germanium (Ge). The first to fourth lower channel layers 141A, 142A, 143A, and 144A and the first to fourth upper channel layers 141B, 142B, 143B, and 144B may be formed of the same material as that of the substrate 101, for example. The number of the first to fourth lower channel layers 141A, 142A, 143A, and 144A and the first to fourth upper channel layers 141B, 142B, 143B, and 144B and shapes thereof may be varied in some example embodiments.

[0041] The source/drain regions 150 may include lower source/drain regions 150A and upper source/drain regions 150B disposed on the lower source/drain regions 150A.

[0042] The source/drain regions 150 may be provided as a source region or a drain region of a transistor. The source/drain regions 150 may be disposed in recess regions partially recessed into an upper portion of the active region 105 on both sides of the gate structure 160. The source/drain regions 150 may be disposed to cover side surfaces of the lower channel layers 140A and the upper channel layers 140B, respectively. In some example embodiments, the lowermost end of the lower source/drain regions 150A may be disposed on a level lower than a level of the lowermost surface of the lower gate structure 160A.

[0043] The source/drain regions 150 may include a plurality of epitaxial layers, but some example embodiments thereof are not limited thereto. The source/drain regions 150 may be configured as a semiconductor layer including silicon (Si) and/or germanium (SiGe). The source/drain regions 150 may include impurities of different types and/or concentrations. The lower source/drain regions 150A and upper source/drain regions 150B may have different conductivity-types. In some example embodiments, the lower source/drain regions 150A may include N-type doped silicon (Si) and/or the upper source/drain regions 150B may include P-type doped silicon germanium (SiGe). However, some example embodiments thereof are not limited thereto, and in some example embodiments, the lower source/drain regions 150A may

include P-type doped silicon germanium (SiGe) and/or the upper source/drain regions 150B may include N-type doped silicon (Si). In some example embodiments, the source/drain regions 150 may include a plurality of regions including different concentrations of elements and/or doping elements.

[0044] The lower source/drain regions 150A may include a first lower epitaxial layer 150A_1, a second lower epitaxial layer 150A_2, and a third lower epitaxial layer 150A_3. The first lower epitaxial layer 150A_1, the second lower epitaxial layer 150A_2, and the third lower epitaxial layer 150A_3 may include silicon (Si) and may include impurities of different elements and/or concentrations.

[0045] Each of the lower source/drain regions 150A may be spaced apart from each other in the first direction X. The lower source/drain regions 150A may be spaced apart from each other on the first level. The lower source/drain regions 150A may include a first lower epitaxial layer 150A_1 disposed on the active region 105 and containing impurities of the first concentration, a second lower epitaxial layer 150A_2 disposed on the first lower epitaxial layer 150A_1, extending to be in contact with the lower channel layers 140A, and including impurities of a second concentration lower than the first concentration, and a third lower epitaxial layer 150A_3 in contact with the first lower epitaxial layer 150A_1, disposed on the internal surface of the second lower epitaxial layer 150A_2, and including impurities of a third concentration higher than the second concentration. In some example embodiments, the third lower epitaxial layer 150A_3 may be spaced apart from the lower channel layers 140A by the second lower epitaxial layer 150A_2.

[0046] The lower source/drain regions 150A may have an N-type conductivity-type and may be an epitaxially grown layer. For example, the first lower epitaxial layer 150A_1, the second lower epitaxial layer 150A_2, and the third lower epitaxial layer 150A_3 may include one of phosphorus (P) and arsenic (As) as a doping element.

[0047] Each of the upper source/drain regions 150B may be spaced apart from each other in the first direction X and may vertically overlap the lower source/drain regions 150A. Each of the upper source/drain regions 150B may be spaced apart from each other on a second level,

higher than the first level. The upper source/drain regions 150B may include a first upper epitaxial layer 150B_1 and a second upper epitaxial layer 150B_2. The first upper epitaxial layer 150B_1 may be disposed on the barrier layer 170 and may extend to be in contact with the first to fourth upper channel layers 141B, 142B, 143B, and 144B. The first upper epitaxial layer 150B_1 may be in contact with the upper gate structure 160B disposed below each of the first to fourth upper channel layers 141B, 142B, 143B, and 144B. The shape of the first upper epitaxial layer 150B_1 may be changed depending on the shape of the first to fourth upper channel layers 141B, 142B, 143B, and 144B, and the shape of the upper gate structure 160B. The second upper epitaxial layer 150B_2 may be disposed on the first upper epitaxial layer 150B_1. The second upper epitaxial layer 150B_2 may be spaced apart from the barrier layer 170 and the upper channel layers 140B by the first upper epitaxial layer 150B_1. The number of the epitaxial layers and the shape thereof may be varied in some example embodiments.

[0048] The first upper epitaxial layer 150B_1 and the second upper epitaxial layer 150B_2 may include silicon germanium (SiGe) doped with a group 3 element and may have a P-type conductivity-type. For example, the first upper epitaxial layer 150B_1 and the second upper epitaxial layer 150B_2 may be doping elements, and may include one of boron (B), aluminum (Al), gallium (Ga), indium (In) and thallium (Tl). A concentration of germanium (Ge) of the first upper epitaxial layer 150B_1 may be lower than those of the lower sacrificial layers (120A in FIG. 9A), the intermediate sacrificial layer (120B in FIG. 9A), and the sacrificial barrier layer (120D in FIG. 13) before the gate structure 160 is replaced.

[0049] The first upper epitaxial layer 150B_1 may have a lower etch selectivity than those of the lower sacrificial layers (120A in FIG. 9A), the intermediate sacrificial layer (120B in FIG. 9A), and the sacrificial barrier layer (120D in FIG. 13) under specific etching conditions during the manufacturing process. Due to the difference in etch selectivity, the lower sacrificial layers (120A in FIG. 9A), the intermediate sacrificial layer (120B in FIG. 9A), and the sacrificial barrier layer (120D in FIG. 13) may be selectively removed, and a second upper epitaxial layer 150B_2 surrounded by the first upper epitaxial layer 150B_1 may remain. In

some example embodiments, the first upper epitaxial layer 150B_1 and the second upper epitaxial layer 150B_2 may have different germanium (Ge) concentrations. For example, the first upper epitaxial layer 150B_1 may include a first concentration of germanium (Ge). The second upper epitaxial layer 150B_2 may include germanium (Ge) of a second concentration higher than the first concentration. The germanium concentration may increase in the order of the first upper epitaxial layer 150B_1 and the second upper epitaxial layer 150B_2.

[0050] The barrier layer 170 may be in contact with at least one of the lower channel layers 140A and at least one of the upper channel layers 140B. In some example embodiments, the barrier layer 170 may be in contact with the upper surface of the uppermost channel layer 144A of the lower channel layers 140A and the lower surface of the lowermost channel layer 141A of the upper channel layers 140B. For example, the barrier layer 170 may be in contact with the upper surface of the fourth lower channel layer 144A and the lower surface of the first upper channel layer 141B. The barrier layer 170 may be disposed between the upper source/drain regions 150B and the lower source/drain regions 150A. The barrier layer 170 may be spaced apart from the lower gate structure 160A by the lower channel layers 140A and may be spaced apart from the upper gate structure 160B by the upper channel layers 140B. At least a portion of the surface in contact with the barrier layer 170 and the lower source/drain regions 150A or at least a portion of the surface in contact with the barrier layer 170 and the upper source/drain regions 150B may have a curved shape, but some example embodiments thereof are not limited thereto. In some example embodiments, the upper surface of the second region 170B of the barrier layer 170 may have a curved shape curved upwardly, and the lower surface of the second region 170B of the barrier layer 170 may have a curved shape curved downwardly.

[0051] In some example embodiments, the “first portion” and “second portion” in some example embodiments may be referred to as “first region” and “second region,” respectively.

[0052] The barrier layer 170 may include a first region 170A disposed between the uppermost lower channel layer 144A of the lower channel layers 140A and the lowermost upper channel layer 141B of the upper channel layers 140B, and a second region 170B

extending from the first region 170A to a region between the lower source/drain regions 150A and the upper source/drain regions 150B. The barrier layer 170 may be disposed to extend to a region between the lower source/drain regions 150A and the upper source/drain regions 150B. In some example embodiments, at least a portion of the barrier layer 170 may extend from the first region 170A to the second region 170B. The barrier layer 170 may further include a portion extending from a portion in contact with the uppermost lower channel layer 144A and the lowermost upper channel layer 141B to a region between the upper source/drain regions 150B and the lower source/drain regions 150A. The thickness of the barrier layer 170 disposed in the second region 170B may be greater than the thickness of the barrier layer 170 disposed in the first region 170A, but some example embodiments thereof are not limited thereto.

[0053] The contact structure 180 may include a lower contact structure 180A electrically connected to the lower source/drain regions 150A and an upper contact structure 180B electrically connected to the upper source/drain regions 150B.

[0054] The contact structure 180 may be disposed on the source/drain regions 150, and may be disposed to have a longer length in the Y-direction than that of the source/drain regions 150 in some example embodiments. The contact structure 180 may be disposed to be recessed into the source/drain regions 150 to a predetermined (or, alternatively, desired or selected) depth.

[0055] The lower contact structure 180A may penetrate through at least a portion of the substrate 101 and the active region 105 and may be in contact with the lower source/drain regions 150A, and may apply an electrical signal to the lower source/drain regions 150A.

[0056] The upper contact structure 180B may penetrate through at least a portion of the first and second interlayer insulating layers 191 and 192 and may be in contact with the upper source/drain regions 150B, and may apply an electrical signal to the upper source/drain regions 150B.

[0057] The contact structure 180 may include a metal silicide layer (not shown) disposed on the lower end including the lower surface, and may further include a barrier layer forming

the side surfaces of the contact structure 180 and extending to the upper surface of the metal silicide layer. The barrier layer may include, for example, a metal nitride such as titanium nitride (TiN), tantalum nitride (TaN), or tungsten nitride (WN). The contact structure 180 may include, for example, a metal material such as aluminum (Al), tungsten (W), or molybdenum (Mo). In some example embodiments, the number of the conductive layers included in the contact structure 180 and the arrangement thereof may be varied.

[0058] The gate contact structure 190 may include a lower gate contact structure 190A and an upper gate contact structure 190B. The lower gate contact structure 190A may be in contact with the lower gate electrode 163A, and the upper gate contact structure 190B may be in contact with the upper gate electrode 163B. The gate contact structure 190 may have a shape and material similar to those of the contact structure 180, but some example embodiments thereof are not limited thereto. In some example embodiments, each of the lower and upper gate contact structures 190A and 190B may include a lower gate contact barrier layer 190A_1 and an upper gate contact barrier layer 190B_1.

[0059] The first to fifth interlayer insulating layers 191, 192, 193, 194, and 195 may include, for example, at least one of an oxide, a nitride, an oxynitride, and a low-κ dielectric. The first to third interlayer insulating layers 191, 192, and 193 may be disposed to cover the upper source/drain regions 150B and the upper gate structure 160B. The fourth and fifth interlayer insulating layers 194 and 195 may be disposed to cover the substrate 101 and the active region 105.

[0060] In some example embodiments, first wiring M1 may include a first upper metal wiring M1a and a second upper metal wiring M1b, and the second wiring M2 may include a first lower metal wiring M2a and a second lower metal wiring M2b. The first upper metal wiring M1a may be electrically connected to the upper source/drain regions 150B through the upper contact structure 180B, and the second upper metal wiring M1b may be electrically connected to the upper gate electrode 163B through the upper gate contact structure 190B. The first lower metal wiring M2a may be electrically connected to the lower source/drain regions 150A through the lower contact structure 180A, and the second lower metal wiring

M2b may be electrically connected to the lower gate electrode 163A through the lower gate contact structure 190A.

[0061] In the description of example embodiments below, descriptions overlapping those described above with reference to FIGS. 1 to 2B will not be provided.

[0062] FIGS. 3A and 3B are cross-sectional diagrams illustrating a semiconductor device 100A in some example embodiments, illustrating regions corresponding to FIGS. 2A and 2B, respectively.

[0063] Referring to FIGS. 3A and 3B, a thickness of the lowermost gate electrode 163A of the lower gate structure 160A of the semiconductor device 100A may be different from the other example embodiments. For example, the thickness of the lowermost gate electrode 163A of the lower gate structure 160A of the semiconductor device 100A may be larger than (e.g., two times or more) a thickness of the lowermost gate electrode 163A of the lower gate structure 160A of the semiconductor devices 100, 100B, etc. from the other example embodiments In some example embodiments, the thickness of the lowermost gate structure 160A disposed below the first lower channel layer 141A may be greater than the thickness of the lower gate structure 160A disposed below the second to fourth lower channel layers 142A, 143A, and 144A. As illustrated in FIGS. 9A and 9B, by increasing the thickness of the lowermost sacrificial layer 120A, the semiconductor device 100A may be provided. Accordingly, in a subsequent process of forming the lower gate contact structure 190A, a contact margin between the lower gate contact structure 190A and the lower gate electrode 163A may be secured.

[0064] In some example embodiments, similar to the thickness of the lowermost gate electrode 163A of the lower gate structure 160A of the semiconductor device 100A, a thickness of first lower epitaxial layer 150A_1 of the semiconductor device 100A may be different (for example, larger) from the other example embodiments.

[0065] FIG. 4 is a cross-sectional diagram illustrating a semiconductor device 100B according to some example embodiments, illustrating a region corresponding to FIG. 2A.

[0066] Referring to FIG. 4, an air gap 170V disposed between the lower source/drain regions

150A and the upper source/drain regions 150B and disposed on the side surface of the barrier layer 170 on the second region 170B may be further included. The air gap 170V, for example, may include air or a gas formed of a material used in a process of manufacturing the semiconductor device 100B.

[0067] FIG. 5 is a cross-sectional diagram illustrating a semiconductor device 100C according to some example embodiments, illustrating a region corresponding to FIG. 2A.

[0068] Referring to FIG. 5, the semiconductor device 100C may further include internal spacers 130 disposed between the lower gate structure 160A and the lower source/drain regions 150A and/or between the upper gate structure 160B and the upper source/drain regions 150B in the first direction X.

[0069] The internal spacers 130 may include lower internal spacers 130A and upper internal spacers 130B. The lower internal spacers 130A may be disposed parallel to the lower gate electrode 163A between the first to fourth lower channel layers 141A, 142A, 143A, and 144A in the Z-direction. For example, the lower internal spacers 130A may separate or completely separate the first to fourth lower channel layers 141A, 142A, 143A, and 144A in the Z-direction. The upper internal spacers 130B may be disposed parallel to the upper gate electrode 163B between the first to fourth upper channel layers 141B, 142B, 143B, and 144B in the Z-direction. The lower gate electrode 163A and the upper gate electrode 163B may be stably spaced apart from the source/drain regions 150 by the lower internal spacers 130A and the upper internal spacers 130B, respectively, and may be electrically isolated from each other. A side surface of the internal spacers 130 opposing the lower gate electrode 163A and the upper gate electrode 163B may have a rounded shape, rounded toward the internal side toward the lower gate electrode 163A and the upper gate electrode 163B, but some example embodiments thereof are not limited thereto. The internal spacers 130 may be formed of oxides, nitrides and/or oxynitrides, and may be, for example, formed of low-κ films. However, in some example embodiments, the internal spacers 130 may not be provided, or only the lower internal spacers 130A may be provided, or only the upper internal spacers 130B may be provided.

[0070] FIG. 6 is a cross-sectional diagram illustrating a semiconductor device 100D according to some example embodiments, illustrating a region corresponding to FIG. 2A.

[0071] Referring to FIG. 6, a lower contact structure 180A may be formed in a region corresponding to the first lower epitaxial layer 150A_1 in FIG. 2A. In the process of forming the lower source/drain regions 150A, the first lower epitaxial layer 150A_1 may be formed of a material including silicon germanium. Thereafter, in the process of forming the lower contact structure 180A, the lower contact structure 180A in a region corresponding to the first lower epitaxial layer 150A_1 in FIG. 2A may be formed by selectively removing the first lower epitaxial layer 150A_1.

[0072] FIG. 7 is a cross-sectional diagram illustrating a semiconductor device 100E according to some example embodiments, illustrating a region corresponding to FIG. 2A.

[0073] Referring to FIG. 7, at least a portion of the interface between the barrier layer 170 and the upper source/drain regions 150B or the interface between the barrier layer 170 and the lower source/drain regions 150A may have a (111) crystal orientation. This may be because at least a portion of the lower surface or upper surface of the sacrificial barrier layer 120D has a (111) crystal orientation in a subsequent process of forming the sacrificial barrier layer 120D. The barrier layer 170 may be spaced apart from the second upper epitaxial layer 150B_2.

[0074] FIG. 8A is a cross-sectional diagram illustrating a semiconductor device 100F according to some example embodiments, illustrating a region corresponding to FIG. 2A.

[0075] Referring to FIG. 8A, a surface on which the barrier layer and the upper source/drain regions are in contact with each other may have a downwardly curved shape. The surface in contact with the barrier layer and the lower source/drain regions may have a downwardly curved shape, but some example embodiments thereof are not limited thereto and the surface may have an upwardly curved shape.

[0076] FIG. 8B is a cross-sectional diagram illustrating a semiconductor device 100G according to some example embodiments, illustrating a region corresponding to FIG. 2A.

[0077] Referring to FIG. 8B, differently from the semiconductor device 100 in FIG. 2A, in

a process of forming a lower contact structure 180A and a lower gate contact structure 190A, both the substrate 101 and the active region 105 may be removed, thereby providing the semiconductor device 100G. Accordingly, the substrate 101 and the active region 105 may be removed, the fourth interlayer insulating layer 194 may be formed, and thereafter, the lower contact structure 180A and the lower gate contact structure 190A may be formed.

[0078] FIGS. 9A, 9B, 10A, 10B, 11, 12, 13, 14, 15A, 15B, 16A, 16B, 17A, 17B, 18A, 18B, 19A, 19B, 20A, 20B, 21A and 21B are cross-sectional diagrams illustrating processes of a method of manufacturing a semiconductor device in order according to some example embodiments. FIGS. 9A, 10A, 11, 12, 13, 14, 15A, 16A, 17A, 18A, 19A, 20A, and 21A illustrate cross-sections corresponding to FIG. 2A, and FIGS. 9B, 10B, 15B, 16B, 17B, 18B, 19B, 20B, and 21B illustrate cross-sections corresponding to FIG. 2B.

[0079] Referring to FIGS. 9A and 9B, sacrificial layers 120, first to fourth lower channel layers 141A, 142A, 143A, and 144A, and first to fourth upper channel layers 141B, 142B, 143B, and 144B may be alternately stacked.

[0080] The sacrificial layers 120 may include lower sacrificial layers 120A, intermediate sacrificial layers 120B, and upper sacrificial layers 120C. The lower sacrificial layers 120A may be replaced with a lower gate dielectric layer 162A and a lower gate electrode 163A as illustrated in FIG. 2A through a subsequent process. The intermediate sacrificial layers 120B may be replaced with a barrier layer 170 as illustrated in FIG. 2A through a subsequent process. The upper sacrificial layers 120C may be replaced with an upper gate dielectric layer 162B and an upper gate electrode 163B as illustrated in FIG. 2A through a subsequent process.

[0081] The sacrificial layers 120 may be formed of a material having etching selectivity with respect to first to fourth lower channel layers 141A, 142A, 143A, and 144A and first to fourth upper channel layers 141B, 142B, 143B, and 144B. The first to fourth lower channel layers 141A, 142A, 143A, and 144A and the first to fourth upper channel layers 141B, 142B, 143B, and 144B may include materials different from those of the sacrificial layers 120. In some example embodiments, the first to fourth lower channel layers 141A, 142A, 143A, and 144A and the first to fourth upper channel layers 141B, 142B, 143B, and 144B may include silicon

(Si), and the sacrificial layers 120 may include silicon germanium (SiGe).

[0082] The lower sacrificial layers 120A, the intermediate sacrificial layers 120B, and the upper sacrificial layers 120C may be formed of materials having etching selectivity with respect to each other. The lower sacrificial layers 120A, the intermediate sacrificial layers 120B, and the upper sacrificial layers 120C may include different concentrations of germanium. In some example embodiments, the lower sacrificial layers 120A may include germanium of a first concentration, the intermediate sacrificial layers 120B may include germanium of a second concentration lower than the first concentration, and the upper sacrificial layers 120C may include germanium of a third concentration lower than the second concentration. In some example embodiments, the concentration of germanium of each of the lower sacrificial layers 120A may be exactly or about 45 at% to exactly or about 60a%, the concentration of germanium of the intermediate sacrificial layer 120B may be exactly or about 30 at% to exactly or about 45 at%, and the concentration of germanium of each of the upper sacrificial layers 120C may be exactly or about 5 at% to exactly or about 30 at%. Specifically, the concentration of germanium of each of the lower sacrificial layers 120A may be exactly or about 50 at%, the concentration of germanium of the intermediate sacrificial layer 120B may be exactly or about 35 at%, and the concentration of germanium of each of the upper sacrificial layers 120C may be exactly or about 15 at%.

[0083] The sacrificial layers 120, the first to fourth lower channel layers 141A, 142A, 143A, and 144A and the first to fourth upper channel layers 141B, 142B, 143B, and 144B may be formed by performing an epitaxial growth process using the substrate 101 as a seed. Each of the sacrificial layers 120, the first to fourth lower channel layers 141A, 142A, 143A, and 144A, and the first to fourth upper channel layers 141B, 142B, 143B, and 144B may have a thickness ranging from exactly or about 1 Å to exactly or about 100 nm. The number of the first to fourth lower channel layers 141A, 142A, 143A, and 144A and the first to fourth upper channel layers 141B, 142B, 143B, and 144B alternately stacked with the sacrificial layers 120 may be varied in some example embodiments.

[0084] Referring to FIGS. 10A and 10B, active structures may be formed by removing a

portion of the sacrificial layers 120, the first to fourth lower channel layers 141A, 142A, 143A, and 144A, the first to fourth upper channel layers 141B, 142B, 143B, and 144B, and the substrate 101, and the sacrificial gate structures 200 and the gate spacers 164 may be formed on the active structures.

[0085] The active structure may include the sacrificial layers 120, the first to fourth lower channel layers 141A, 142A, 143A, and 144A, and the first to fourth upper channel layers 141B, 142B, 143B, and 144B alternately stacked with each other, and may further include an active region 105 formed such that a portion of the substrate 101 is removed and protrudes to the upper surface of the substrate 101. The active structures may be formed in a line form extending in one direction, for example, the X-direction, and may be spaced apart from each other in the Y-direction.

[0086] In a region from which a portion of the substrate 101 is removed, by filling an insulating material and recessing the active region 105 to protrude, a device isolation layer 110 may be formed. An upper surface of the device isolation layer 110 may be formed lower than an upper surface of the active region 105.

[0087] The sacrificial gate structures 200 may be a sacrificial structure formed in the region in which the upper gate dielectric layer 162B and the upper gate electrode 163B are disposed on the channel structure 140 through a subsequent process as illustrated in FIG. 2A. The sacrificial gate structures 200 may include first and second sacrificial gate layers 202 and 205, and a mask pattern layer 206 stacked in order. The first and second sacrificial gate layers 202 and 205 may be patterned using a mask pattern layer 206. The first and second sacrificial gate layers 202 and 205 may be an insulating layer and a conductive layer, respectively. For example, the first sacrificial gate layer 202 may include silicon oxide, and the second sacrificial gate layer 205 may include polysilicon. The mask pattern layer 206 may include silicon nitride. The sacrificial gate structures 200 may have a line shape extending in one direction by intersecting the active structures. The sacrificial gate structures 200 may, for example, extend in the Y-direction and may be spaced apart from each other in the X-direction.

[0088] Gate spacers 164 may be formed on both sidewalls of sacrificial gate structures 200. The gate spacers 164 may be formed by forming a film having a uniform thickness along the upper and side surfaces of the sacrificial gate structures 200 and the active structures and performing anisotropic etching. The gate spacers 164 may be formed of a low-κ material, and may include, for example, at least one of SiO, SiN, SiCN, SiOC, SiON, and SiOCN.

[0089] Referring to FIG. 11, by forming the recess regions RC by removing the exposed sacrificial layers 120, the first to fourth lower channel layers 141A, 142A, 143A, and 144A, and the first to fourth upper channel layers 141B, 142B, 143B, and 144B between the sacrificial gate structures 200, the channel structure 140 may be formed.

[0090] The exposed sacrificial layers 120, the first to fourth lower channel layers 141A, 142A, 143A, and 144A, and the first to fourth upper channel layers 141B, 142B, 143B, and 144B may be removed using the sacrificial gate structures 200 and the gate spacers 164 as masks. The remaining sacrificial layers 120 may be selectively etched with respect to the channel structure 140 by, for example, a wet etching process, may be removed to a predetermined (or, alternatively, desired or selected) depth from the side surface in the X-direction, and may have side surfaces curved internally. The side surfaces of the sacrificial layers 120, the first to fourth lower channel layers 141A, 142A, 143A, and 144A, and the first to fourth upper channel layers 141B, 142B, 143B, and 144B may be formed to be coplanar with each other in a direction perpendicular to the upper surface of the substrate 101. However, the shapes of the side surfaces of the sacrificial layers 120, the first to fourth lower channel layers 141A, 142A, 143A, and 144A, and the first to fourth upper channel layers 141B, 142B, 143B, and 144B are not limited to the illustrated examples. The remaining side surfaces of the first to fourth lower channel layers 141A, 142A, 143A, and 144A and the first to fourth upper channel layers 141B, 142B, 143B, and 144B may be etched in the X-direction and may have an outwardly curved side surface.

[0091] Referring to FIG. 12, the lower source/drain regions 150A may be formed by forming an epitaxial layer in the first recess region RC1.

[0092] The lower source/drain regions 150A may be formed by epitaxial growth, and may

extend to be in contact with the first to fourth lower channel layers 141A, 142A, 143A, and 144A and the lower sacrificial layers 120A in the first recess region RC1. The upper surface of the lower source/drain regions 150A may have a downwardly curved shape, but some example embodiments thereof are not limited thereto.

[0093] The lower source/drain regions 150A may include impurities, which, for example, may be formed by in-situ doping. In some example embodiments, the first lower epitaxial layer 150A_1 may include impurities in a first concentration, the second lower epitaxial layer 150A_2 may include impurities in a second concentration lower than the first concentration, and the third lower epitaxial layer 150A_2 may include impurities at a higher third concentration than the second concentration. The third concentration may be higher than the first concentration, but some example embodiments thereof are not limited thereto.

[0094] Referring to FIG. 13, in the second recess region RC2, a sacrificial barrier layer 120D may be formed on the lower source/drain regions 150A.

[0095] The sacrificial barrier layer 120D may be formed by epitaxial growth. The sacrificial barrier layer 120D may be formed of a material having etching selectivity with respect to the lower sacrificial layers 120A and the upper sacrificial layers 120C. In some example embodiments, the sacrificial barrier layer 120D may include silicon germanium (SiGe). For example, the sacrificial barrier layer 120D may include germanium in a concentration equal or substantially equal to or higher than the concentration of germanium included in the intermediate sacrificial layers 120B. The sacrificial barrier layer 120D may include germanium in a lower concentration than the concentration of germanium included in the lower sacrificial layers 120A to have etching selectivity with respect to the lower sacrificial layers 120A and the upper sacrificial layers 120C, and may include germanium in a higher concentration than the concentration of germanium included in the upper sacrificial layers 120C.

[0096] At least a portion of the lower surface or the upper surface of the sacrificial barrier layer 120D may have a (111) crystal orientation, but some example embodiments thereof are not limited thereto.

[0097] Referring to FIG. 14, in the third recess region RC3, upper source/drain regions 150B may be formed on the sacrificial barrier layer 120D.

[0098] The upper source/drain regions 150B may be formed by epitaxial growth, and may extend to be in contact with the first to fourth upper channel layers 141B, 142B, 143B, and 144B and the upper sacrificial layers 120C in the third recess region RC3. The lower surface of the upper source/drain regions 150A may have an upwardly curved shape, but some example embodiments thereof are not limited thereto.

[0099] The upper source/drain regions 150B may include impurities by in-situ doping. The first upper epitaxial layer 150B_1 and the second upper epitaxial layer 150B_2 may include silicon germanium (SiGe). In some example embodiments, the second upper epitaxial layer 150B_2 may include germanium in a higher concentration than the concentration of germanium included in the first upper epitaxial layer 150B_1. Since the first upper epitaxial layer 150B_1 has etching selectivity in the subsequent process of removing the intermediate sacrificial layer 120B and the sacrificial barrier layer 120D, the first upper epitaxial layer 150B_1 may include germanium in a lower concentration than the concentration of germanium of each included in the intermediate sacrificial layer 120B and the sacrificial barrier layer 120D.

[00100] Referring to FIGS. 15A and 15B, a first interlayer insulating layer 191 may be formed and the sacrificial gate structures 200 may be removed.

[00101] The first interlayer insulating layer 191 may be formed by forming an insulating film covering the sacrificial gate structures 200 and the upper source/drain regions 150B and performing a planarization process.

[00102] The sacrificial gate structures 200 may be selectively removed with respect to the gate spacers 164, the first interlayer insulating layer 191, the first to fourth lower channel layers 141A, 142A, 143A, and 144A, and the first to fourth upper channel layers 141B, 142B, 143B, and 144B. Accordingly, the upper gap regions UR may be formed by removing the sacrificial gate structures 200.

[00103] Referring to FIGS. 16A and 16B, the first lower gap regions LR1 may be formed

by removing the lower sacrificial layers 120A.

[00104] Since the lower sacrificial layers 120A may have etching selectivity with respect to the intermediate sacrificial layer 120B, the upper sacrificial layers 120C, the first to fourth lower channel layers 141A, 142A, 143A, and 144A, and the first to fourth upper channel layers 141B, 142B, 143B, and 144B, the lower sacrificial layers 120A may be selectively etched. For example, when the lower sacrificial layers 120A include silicon germanium (SiGe) and the first to fourth lower channel layers 141A, 142A, 143A, and 144A include silicon (Si), the lower sacrificial layers 120A may be selectively removed by performing a wet etching process using peracetic acid as an etchant.

[00105] Referring to FIGS. 17A and 17B, a lower gate structure 160A may be formed in the first lower gap regions LR1. Second lower gap regions LR2 may be formed by removing the intermediate sacrificial layer 120B and the sacrificial barrier layer 120D.

[00106] The lower gate dielectric layer 162A may be formed to conformally cover internal surfaces of the first lower gap regions LR1. The lower gate electrode 163A may be formed to completely fill the first lower gap regions LR1. Accordingly, a lower gate structure 160A including a lower gate dielectric layer 162A and a lower gate electrode 163A may be formed.

[00107] Since the intermediate sacrificial layer 120B and the sacrificial barrier layer 120D may have etching selectivity with respect to the lower source/drain regions 150A, the upper source/drain regions 150B, the upper sacrificial layers 120C, the first to fourth lower channel layers 141A, 142A, 143A, and 144A, and the first to fourth upper channel layers 141B, 142B, 143B, and 144B, the intermediate sacrificial layer 120B and the sacrificial barrier layer 120D may be selectively etched. Accordingly, the second lower gap regions LR2 may be formed. In this case, the first interlayer insulating layer 191 and the gate spacers 164 may support the lower channel layers 140A and the upper channel layers 140B.

[00108] Referring to FIGS. 18A and 18B, a barrier layer 170 may be formed in the second lower gap regions LR2. third lower gap regions LR3 may be formed by removing the upper sacrificial layers 120C.

[00109] A barrier layer 170 may be formed in the second lower gap regions LR2 such that

the lower source/drain regions 150A and the upper source/drain regions 150B may not be in contact with each other. The barrier layer 170 may isolate the lower source/drain regions 150A and the upper source/drain regions 150B from each other. When the second lower gap regions LR2 are not completely filled, an air gap 170V may be formed as in the semiconductor device 100B in FIG. 4.

[00110] Referring to FIGS. 19A and 19B, an upper gate structure 160B may be formed in the upper gap regions UR and the third lower gap regions LR3.

[00111] The upper gate dielectric layer 162B may be formed to conformally cover internal surfaces of the third lower gap regions LR3. The upper gate electrode 163B may be formed to completely fill the upper gap regions UR and the third lower gap regions LR3. Accordingly, an upper gate structure 160B including an upper gate dielectric layer 162B, an upper gate electrode 163B, and gate spacers 164 may be formed.

[00112] Referring to FIGS. 20A and 20B, an upper contact structure 180B, an upper gate contact structure 190B, and first wiring M1 may be formed.

[00113] A second interlayer insulating layer 192 and a third interlayer insulating layer 193 covering the first interlayer insulating layer 191 and the upper gate structure 160B may be formed.

[00114] An upper contact structure 180B may be formed to penetrate through at least a portion of the first and second interlayer insulating layers 191 and 192 and to be in contact with the upper source/drain regions 150B.

[00115] An upper gate contact structure 190B may be formed to penetrate through at least a portion of the second interlayer insulating layer 192 and be in contact with the upper gate electrode 163B.

[00116] By forming a first upper metal wiring M1a and a second upper metal wiring M1b to penetrate through at least a portion of the third interlayer insulating layer 193 and the third interlayer insulating layer 193 on the upper contact structure 180B and the upper gate contact structure 190B and to be in contact with the upper contact structure180B and the upper gate contact structure 190B, respectively, the first upper metal wiring M1 may be formed.

[00117] Referring to FIGS. 21A and 21B, a lower contact structure 180A, a lower gate contact structure 190A, and a second wiring M2 may be formed.

[00118] The bonding layer 300 and the base substrate 400 may be formed on the first metal wiring M1, and the lower contact structure 180A penetrating through at least a portion of the substrate 101 and in contact with the lower source/drain regions 150A may be formed.

[00119] A lower gate contact structure 190A may be formed to penetrate through at least a portion of the substrate 101 and be in contact with the lower gate electrode 163A.

[00120] A fourth interlayer insulating layer 194 may be formed on the substrate 101, and a first lower metal wiring M2a and a second lower metal wiring M2b may be formed to be in contact with the lower contact structure 180A and the lower gate contact structure 190A, respectively, thereby forming the second wiring M2.

[00121] Referring to FIGS. 2A and 2B together, by removing the bonding layer 300 and the base substrate 400, the semiconductor device 100 may be provided.

[00122] According to some example embodiments, in the semiconductor device, by disposing a barrier layer between the lower and upper structures, the lower and upper source/drain regions may be isolated from each other, and the lower and upper source/drain regions may have different conductivity-types. Accordingly, the upper contact structure may be in contact with the upper surface of the upper source/drain region, and the lower contact structure may be in contact with the lower surface of the lower source/drain region, thereby providing a semiconductor device having relatively high integration density.

[00123] When the terms "about" or “substantially” are used in this specification in connection with a numerical value, it is intended that the associated numerical value includes a manufacturing or operational tolerance (e.g., ±10 %) around the stated numerical value. Moreover, when the words "generally" and "substantially" are used in connection with geometric shapes, it is intended that precision of the geometric shape is not required but that latitude for the shape is within the scope of the disclosure. Further, regardless of whether numerical values or shapes are modified as "about" or "substantially," it will be understood that these values and shapes should be construed as including a manufacturing or operational

tolerance (e.g., ±10 %) around the stated numerical values or shapes.

[00124] While the example embodiments have been illustrated and described above, it will be configured as apparent to those skilled in the art that modifications and variations could be made without departing from the scope of the present disclosure as defined by the appended claims.

What Is Claimed Is:

1. A semiconductor device, comprising:

a lower structure;

a barrier layer on the lower structure; and

an upper structure on the barrier layer,

the lower structure including

lower source/drain regions spaced apart from each other in a first direction;

lower active layers spaced apart from each other in a vertical direction, between the lower source/drain regions, and connected to the lower source/drain regions; and

a lower gate structure extending in a second direction perpendicular to the first direction and including portions below each of the lower active layers,

the upper structure including

upper source/drain regions spaced apart from each other in the first direction and vertically overlapping the lower source/drain regions;

upper active layers spaced apart from each other in the vertical direction, between the upper source/drain regions, connected to the upper source/drain regions, and vertically overlapping the lower active layers; and

an upper gate structure extending in the second direction, including portions on each of the upper active layers, and vertically overlapping the lower gate structure, and

an uppermost lower active layer of the lower active layers and a lowermost upper active layer of the upper active layers being in contact with the barrier layer.

2. The semiconductor device of claim 1, wherein

the lower active layers include a lowermost lower active layer, the uppermost lower active layer, and one or more first lower active layers between the lowermost lower active layer and the uppermost lower active layer,

the upper active layers include the lowermost upper active layer, an uppermost upper

active layer, and one or more first upper active layers between the lowermost upper active layer and the uppermost upper active layer,

the lower gate structure surrounds a lower surface, an upper surface, and a side surface of each of the one or more first lower active layers and the lowermost lower active layer, and covers a lower surface and a side surface of the uppermost lower active layer, in the second direction, and

the upper gate structure surrounds a lower surface, an upper surface, and a side surface of each of the one or more first upper active layers and the uppermost upper active layer, and covers an upper surface and a side surface of the lowermost upper active layer, in the second direction.

3. The semiconductor device of claim 1 or claim 2, wherein the upper source/drain regions and the lower source/drain regions have different conductivity-types.

4. The semiconductor device of any one of claims 1 to 3, wherein the barrier layer further includes a portion extending from a portion in contact with the uppermost lower active layer and the lowermost upper active layer to a region between the upper source/drain regions and the lower source/drain regions.

5. The semiconductor device of claim 4, wherein

the barrier layer is in contact with the upper source/drain regions and the lower source/drain regions, and

at least a portion of an interface between the barrier layer and the upper source/drain regions or an interface between the barrier layer and the lower source/drain regions has a (111) crystal orientation.

6. The semiconductor device of claim 4, wherein

the barrier layer is in contact with the upper source/drain regions and the lower

source/drain regions, and

at least one of at least a portion of an interface between the barrier layer and the lower source/drain regions and at least a portion of an interface between the barrier layer and the upper source/drain regions have a curved shape.

7. The semiconductor device of any one of claims 1 to 6, further comprising:

internal spacers between the lower gate structure and the lower source/drain regions or between the upper gate structure and the upper source/drain regions in the first direction.

8. The semiconductor device of any one of claims 1 to 7, wherein a lowermost end of the lower source/drain regions is on a level lower than a level of a lowermost surface of the lower gate structure.

9. The semiconductor device of claim 1, wherein, among the portions of the lower gate structure below the lower active layers, respectively, a thickness of a portion of the lower gate structure below a lowermost lower active layer among the lower active layers is greater than a thickness of each of the other portions of the lower structure.

10. The semiconductor device of any one of claims 1 to 9, wherein

each of the upper source/drain regions includes:

a first upper epitaxial layer on the barrier layer, extending to be in contact with the upper active layers, and including germanium (Ge) of a first concentration; and

a second upper epitaxial layer on the first upper epitaxial layer and including germanium (Ge) of a second concentration higher than the first concentration, and

the second upper epitaxial layer is spaced apart from the barrier layer and the upper active layers by the first upper epitaxial layer.

11. The semiconductor device of any one of claims 1 to 10, wherein

each of the lower source/drain regions includes:

a first lower epitaxial layer including first concentration impurities;

a second lower epitaxial layer on the first lower epitaxial layer, extending to be in contact with the lower active layers, and including impurities of a second concentration lower than the first concentration; and

a third lower epitaxial layer in contact with the first lower epitaxial layer, on an internal surface of the second lower epitaxial layer, and including impurities of a third concentration higher than the second concentration, and

the third lower epitaxial layer is spaced apart from the lower active layers by the second lower epitaxial layer.

12. The semiconductor device of any one of claims 1 to 11, further comprising:

an upper contact structure on the upper source/drain regions and connected to the upper source/drain regions; and

a lower contact structure below the lower source/drain regions and connected to the lower source/drain regions.

13. The semiconductor device of any one of claims 1 to 12, further comprising:

an upper gate contact structure on the upper gate structure and electrically connected to a gate electrode of the upper gate structure; and

a lower gate contact structure below the lower gate structure and electrically connected to a lower gate electrode of the lower gate structure.

14. A semiconductor device, comprising:

a first structure;

a barrier layer on the first structure; and

a second structure on the barrier layer,

the first structure including

first source/drain regions spaced apart from each other in a first direction;

first channel layers spaced apart from each other in a vertical direction, between the first source/drain regions, and connected to the first source/drain regions; and

a first gate structure extending in a second direction perpendicular to the first direction and including portions below the first channel layers, respectively,

the second structure including

second source/drain regions spaced apart from each other in the first direction;

second channel layers spaced apart from each other in the vertical direction, between the second source/drain regions, and connected to the second source/drain regions; and

a second gate structure extending in the second direction and including portions on the second channel layers, respectively,

the barrier layer including a first portion between an uppermost first channel layer among the first channel layers and a lowermost second channel layer among the second channel layers, and a second portion extending from the first portion to a region between the first source/drain regions and the second source/drain regions, and

at least one of an upper surface and a lower surface of the second portion having a curved shape.

15. The semiconductor device of claim 14, further comprising:

an air gap between the first source/drain regions and the second source/drain regions and on a side surface of the second portion of the barrier layer.

16. The semiconductor device of claim 14 or claim 15, wherein a thickness of the second portion of the barrier layer is greater than a thickness of the first portion of the barrier layer.

17. The semiconductor device of any one of claims 14 to 16, wherein

the upper surface of the second portion of the barrier layer has an upwardly curved shape, and

the lower surface of the second portion of the barrier layer has a downwardly curved shape.

18. The semiconductor device of any one of claims 14 to 17, wherein

the second source/drain regions include:

a first upper epitaxial layer on the barrier layer, extending to be in contact with the second channel layers, and including germanium (Ge) of a first concentration; and

a second upper epitaxial layer on the first upper epitaxial layer and including germanium (Ge) of a second concentration higher than the first concentration,

the second upper epitaxial layer is spaced apart from the barrier layer and the second channel layers by the first upper epitaxial layer.

19. The semiconductor device of any one of claims 14 to 18, further comprising:

a first contact structure below the first source/drain regions and in contact with the first source/drain regions;

a second contact structure on the second source/drain regions and in contact with the second source/drain regions.

20. A semiconductor device, comprising:

lower channel layers and upper channel layers stacked in a vertical direction;

lower source/drain regions spaced apart from each other on a first level;

upper source/drain regions spaced apart from each other on a second level higher than the first level;

lower channel layers between the lower source/drain regions and spaced apart from

each other in a vertical direction;

upper channel layers between the upper source/drain regions and spaced apart from each other in the vertical direction;

a barrier layer between an uppermost lower channel layer of the lower channel layers and a lowermost upper channel layer of the upper channel layers, and between the lower source/drain regions and the upper source/drain regions;

a lower gate structure below the barrier layer and extending by covering an upper surface, a side surface, and a lower surface of at least one of the lower channel layers;

an upper gate structure on the barrier layer and extending by covering an upper surface, a side surface, and a lower surface of at least one of the upper channel layers;

a lower contact structure below the lower source/drain regions and electrically connected to the lower source/drain regions; and

an upper contact structure on the upper source/drain regions and electrically connected to the upper source/drain regions.