

FIG.1

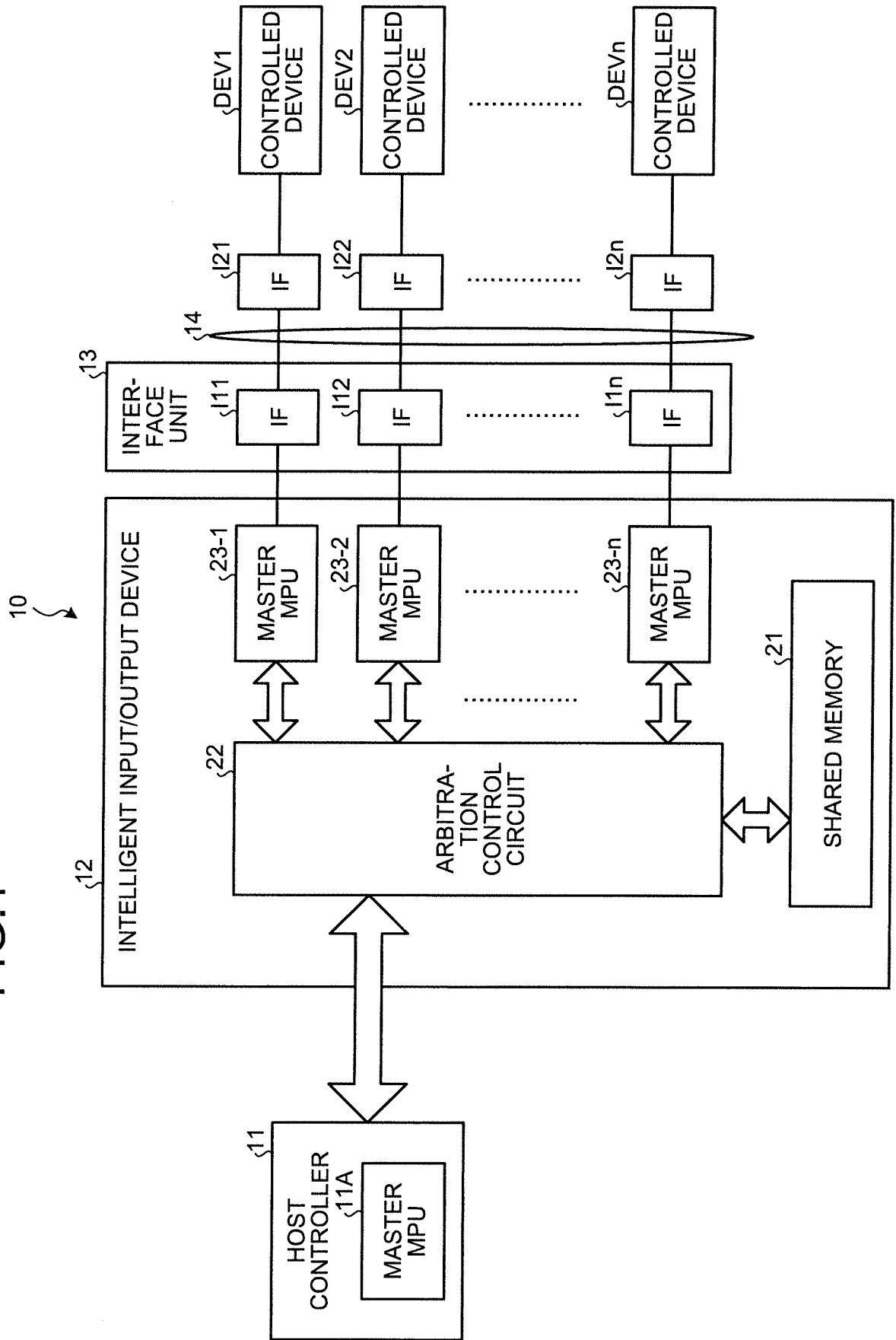


FIG.2

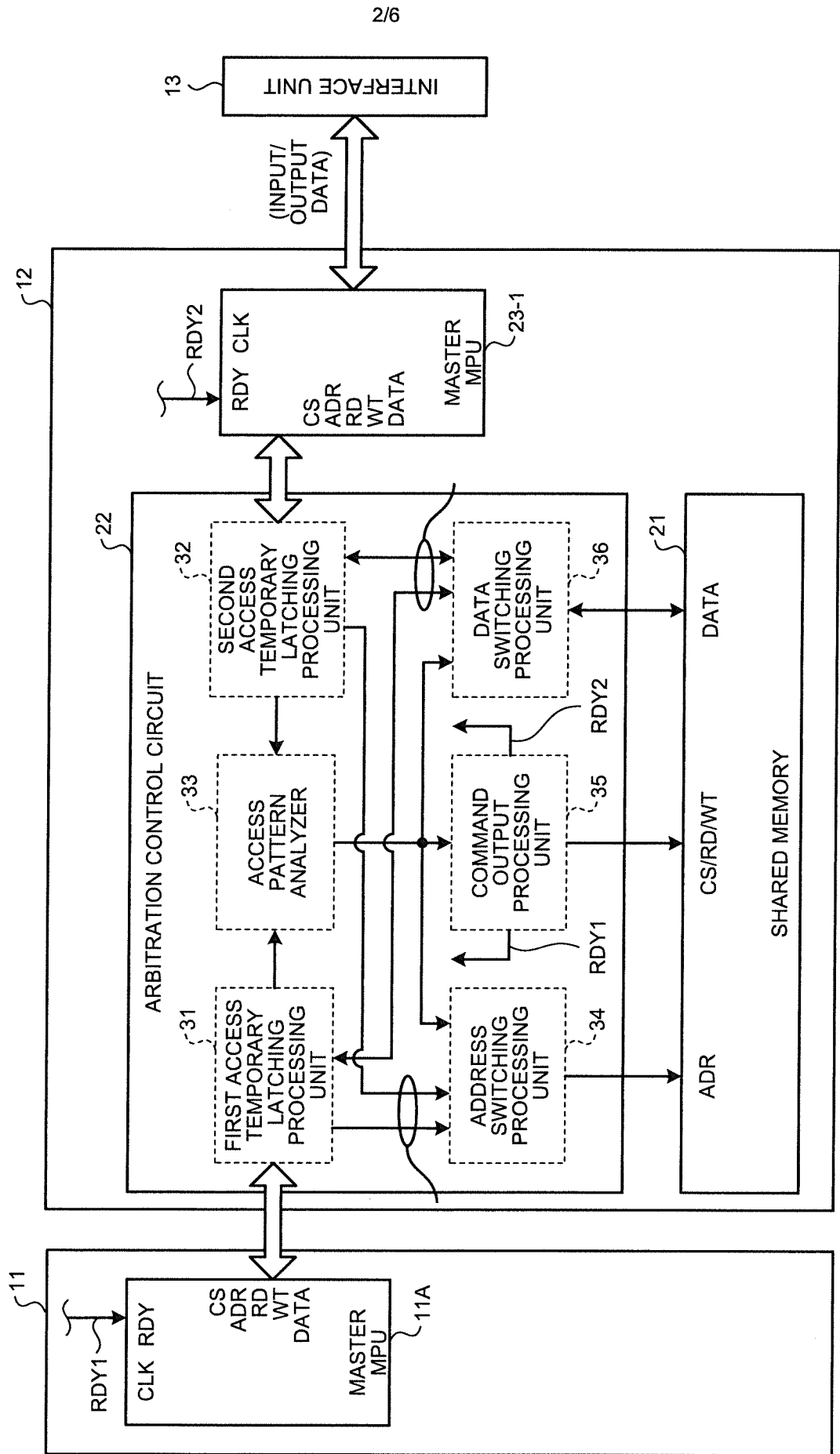


FIG.3

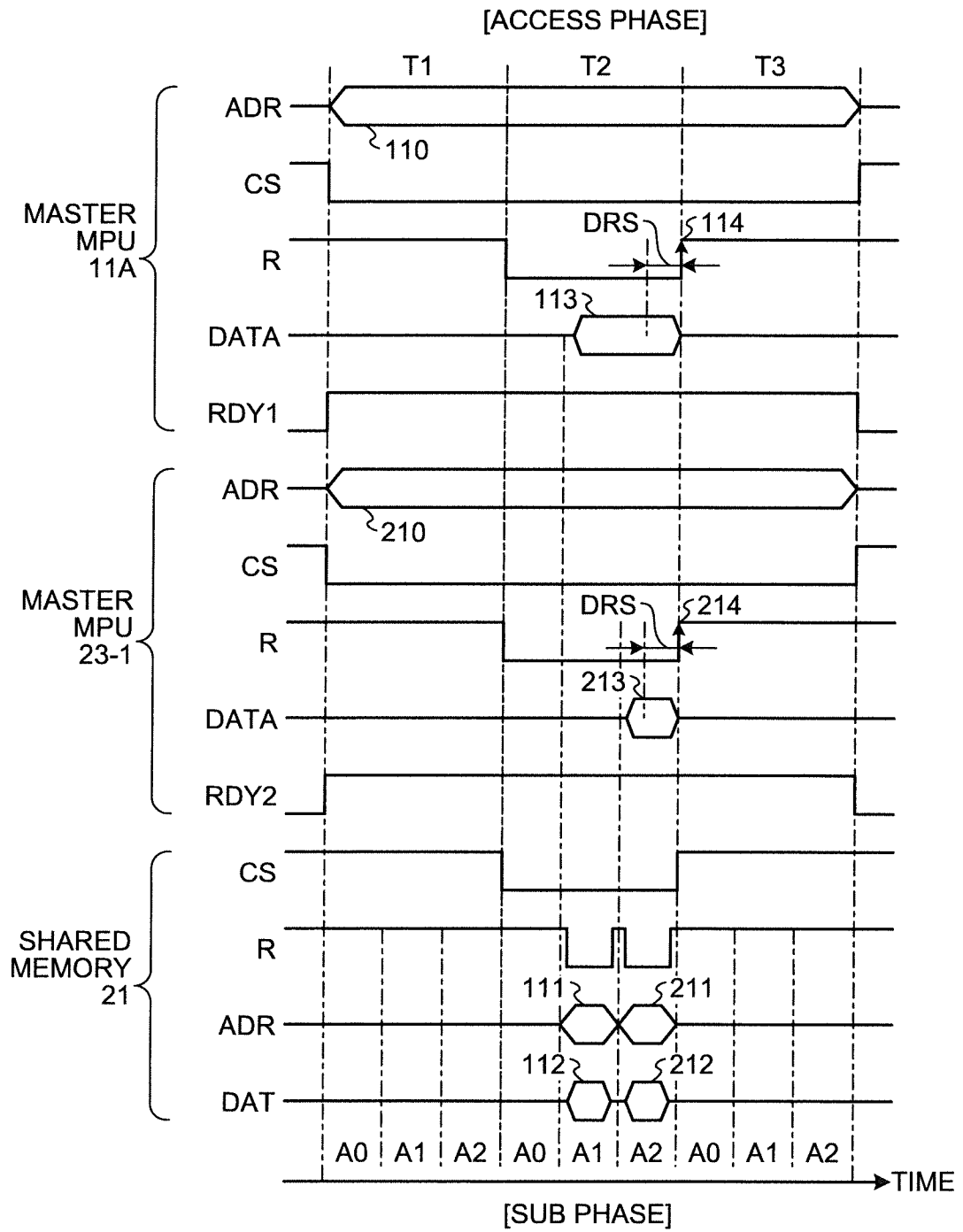


FIG.4

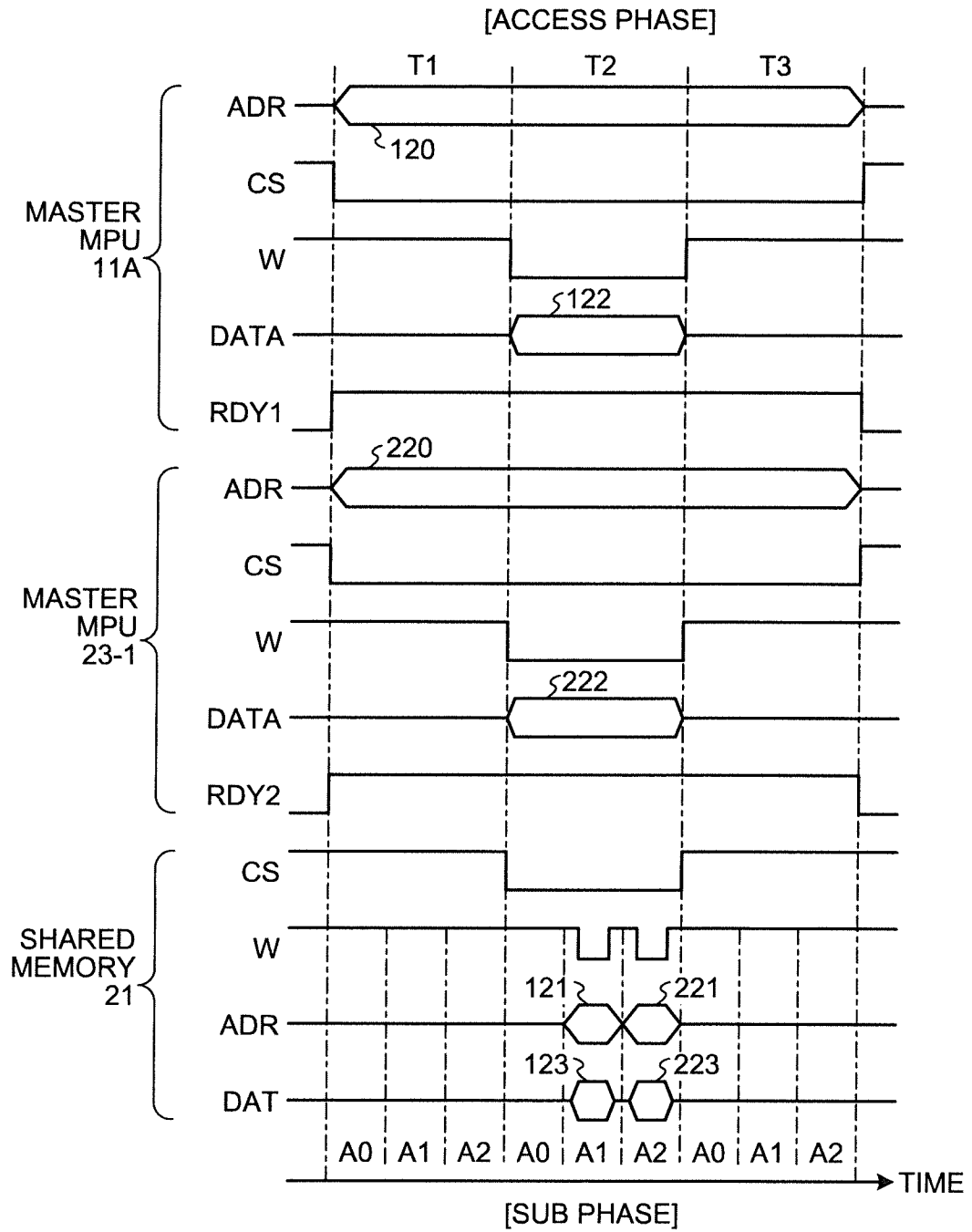


FIG.5

SHARED MEMORY ACCESS PATTERN No.	OVERLAPPING R/W COMMANDS FROM MPU1 AND MPU2									ACCESS TO SHARED MEMORY	
	MPU1 ACCESS				MPU2 ACCESS					T2 PHASE	
	T2 PHASE				T2 PHASE						
	Mode	CS	RD	WT	Mode	CS	RD	WT		A1	A2
1	RD	0	0	1	RD	0	0	1	→	RI1	RI2
2	WT	0	1	0	WT	0	1	0	→	WI1	WI2
3	RD	0	0	1	WT	0	1	0	→	RI1	WI2
4	WT	0	1	0	RD	0	0	1	→	RI2	WI1
5	RD	0	0	1	N	1	1	1	→	RI1	-
5	RD	0	0	1	C	0	1	1	→	RI1	-
6	N	1	1	1	RD	0	0	1	→	RI2	-
6	C	0	1	1	RD	0	0	1	→	RI2	-
7	WT	0	1	0	N	1	1	1	→	WI1	-
7	WT	0	1	0	C	0	1	1	→	WI1	-
8	N	1	1	1	WT	0	1	0	→	WI2	-
8	C	0	1	1	WT	0	1	0	→	WI2	-
9	N	1	1	1	N	1	1	1	→	-	-
9	C	0	1	1	C	0	1	1	→	-	-

Mode RD:READ MODE
WT:WRITE MODE
C:CHIP SELECT MODE
N:NON-OPERATION MODE

FIG. 6

