

A METHOD OF FABRICATING A SEMICONDUCTOR PRESSURE SENSOR

The present invention relates to a method of fabricating a semiconductor pressure sensor.

5 It can be expected that a semiconductor pressure sensor will have the advantages of small size, low cost and a high pressure performance as compared with a mechanical pressure sensor using a Bourdon tube or a bellows. A typical example of a semiconductor pressure sensor is a silicon diaphragm type pressure
10 sensor. The structure of a silicon diaphragm type pressure sensor is disclosed in, for example, "Diaphragm Formation and Pressure Sensitivity in Batch-Fabricated Silicon Pressure Sensors", IEDM Technical Digest, December 1978, pp 96-99. This
15 publication considered the effects of controlling the thickness of the diaphragm of the sensor.

However, little consideration has been given in the art to the effect of the size and shape of the diaphragm, but the inventor of the present invention
20 has found that it is important to make the size and shape of such diaphragms uniform.

When forming such diaphragms, it is usual to use

(15)

an anisotropic etching technique. This is because the thickness of the diaphragm can be controlled easily when using such an etching technique.

In order that uniform strains may be generated in four diffused piezoresistors by pressure applied to a diaphragm, it is desirable that the diaphragm is circular. However, when a silicon (Si) substrate having a (100) crystallographic plane is selectively etched by an anisotropic etching technique, it is difficult to form a completely circular diaphragm because of the effect of the crystallographic direction. This is true even if selective etching is performed using a mask with a circular opening. Thus it is common that the diaphragm structure has an octagonal or similarly polygonal shape. With this polygonal shape, the distance from the center to the periphery of the diaphragm is different at the edges and corners thereof, which means that the strain is likely to be irregular over the diaphragm surface thereby inevitably causing irregularities in the variations of the diffused piezoresistors. There is also the problem that the size and shape of the diaphragm varies in dependence upon the etching time.

The present invention seeks to overcome, or at least ameliorate these problems, by controlling the shape of the diaphragm. Control is achieved by making use of the fact that semiconductor regions of

different impurity concentrations are etched at different rates. The present invention therefore proposes a method of fabricating a semiconductor pressure sensor having a predetermined diaphragm configuration, comprising the steps
5 of:

forming a highly doped region in a single crystal semiconductor substrate with first and second principal planes facing each other by covering a part of the first principal plane by a mask for defining the predetermined
10 diaphragm configuration, and selectively introducing impurities into a part of the substrate which is not covered by the mask;

forming an epitaxial semiconductor region on the second principal plane;

15 forming semiconductor regions for gauge resistors by selectively introducing impurities into the epitaxial semiconductor region; and

etching a part of the first principal plane other than that in which the highly doped region is formed,
20 using the highly doped region as an etching stop thereby to form the predetermined diaphragm configuration such that it is bounded by the highly doped region, whereby a controlled recess providing the predetermined diaphragm configuration, independent of the crystal orientation of the semiconductor substrate, is formed.

25 Thus, in the formation of a semiconductor pressure sensor the part of the substrate to form the diaphragm may remain undoped whilst the surrounding parts may be highly doped. Then the part to form the diaphragm is selectively

12

- 3a -

etched, with the highly doped regions restraining excessive lateral etching. Thus the diaphragm may be formed accurately to a desired shape, e.g. a circle.

5 An embodiment of the present invention will now be described in detail, by way example, with reference to the accompanying drawings, in which:

Figure 1 and Figures 3 to 10 are sections showing steps in a method of fabricating a pressure sensor, being a first embodiment of the present invention,

10 Figures 2 and 11 are perspective views showing

the method of fabricating the pressure sensor of the first embodiment,

Figure 12 is a graph showing the relationship between impurity concentration in a semiconductor substrate and etching rate with anisotropic etching using alkaline etchants;

Figure 13 is a plan view of a completed diaphragm pressure sensor manufactured according to the first embodiment of the present invention, viewed from the plane in which gauge resistors are formed;

Figure 14 is a section taken along the line A-A' of Figure 13; and

Figure 15 is a sectional view showing a semiconductor substrate manufactured according to another embodiment of the present invention.

A first embodiment of the present invention will now be described in detail with reference to Figures 1' to 11.

STEP 1.

A p⁻-type single crystalline silicon substrate (or Si wafer) of a high resistivity is prepared, which contains either a crystal plane (100) or a crystal plane adjacent thereto. As shown in Figures 1 and 2, impurities are selectively introduced into the first principal plane (hereinafter referred to as the reverse surface) of the silicon substrate 11 by deposition or ion implantation using a mask 10. This

(a)

- 5 -

introduction of impurities is an extremely important step in achieving the advantages of the present invention, as will be described subsequently. The impurities used may be either p-type or n-type. In the embodiment now described, impurities with a high diffusion coefficient, such as boron (B) ions, are introduced by ion implantation into a peripheral portion of the substrate 11 surrounding a region 11a (in which a recess will be formed), to provide a p-type, highly doped region 12. The region 11a, in which no impurities are introduced, is formed so as to have e.g. a circular shape. As shown in Figure 2, this is achieved by covering the region 11a with a circular mask 10. It is preferable that the boron ions are implanted with an energy between 75 keV and 125 keV, and that the implanted dose is between 10^{14} atoms/cm² to 10^{16} atoms/cm². The mask 10 may be an insulating film such as SiO₂ film, or alternatively a photoresist film or a silicon nitride film may be used. It is necessary only that the mask 10 is made of a material which blocks the introduction of impurities into the substrate.

STEP 2.

After removal of the mask 10, oxide films 10A and 10B e.g. of SiO₂ are formed over both principal planes of the substrate. N-type impurities such as antimony (Sb) ions are selectively introduced into the second

principal plane (hereinafter referred to as the upper surface) of the substrate adjacent to the region 11 using the oxide film 10A as a mask, as shown in Figure 3, to form an n^+ -type impurity region 13. If the method used for the introduction of the n-type impurities is predeposition, impurities such as Sb_2O_3 may be deposited on the surface of the Si wafer by placing both a solid impurity source of Sb_2O_3 and the Si wafer in a quartz tube, using Argon (Ar) and Oxygen (O_2) as carrier gases, and maintaining a furnace containing the quartz tube at $900^\circ C$. If ion implantation is used, however, the upper surface of the substrate, on which the epitaxial region is to be formed, would be damaged by ions if the ions were implanted to a high density in a single operation. Therefore, ion implantation is carried out with an implantation energy of between 75 keV and 125 keV at a dose of 1×10^{14} atoms/cm², and this ion implantation is repeated 2 or 3 times.

A p-type isolation region 14 is formed separate from, but surrounding, the n^+ -type region 13. The n^+ -type region 13 and the p-type region 14 are formed independently of each other, the order of their formation being unimportant. The p-type isolation region 14 is very useful when a pressure sensor and other circuit elements are to be formed on a single semiconductor substrate.

STEP 3.

To provide drive-in diffusion, heat treatment at a temperature of at least $1,000^{\circ}\text{C}$ is carried out in an oxidizing atmosphere to diffuse a high concentration of impurities into the peripheral portion of the reverse surface of the substrate, as shown in Figure 4, to form a deep p^{+} -type region 12a with an impurity concentration of about 10^{19} atoms/cm².

STEP 4.

After removal of the oxide films 10A and 10B, an n-type Si region 15 having low concentration is formed by epitaxial growth to a thickness of 25 to 30 μm over the upper surface of the substrate, as shown in Figure 5. This epitaxial growth changes the n^{+} -type region 13 of the substrate surface into an n^{+} -type buried region 13A, and the p-type region 14 into a p-type buried region 14a. The epitaxial growth is preferably carried out by the thermal decomposition of silane (SiH_4) at about $1,100^{\circ}\text{C}$.

STEP 5.

As shown in Figure 6, boron ions are selectively diffused into parts of the upper surface of the n-type Si region 15 to create p-type diffused regions 16, which will form gauge resistors. A suitable method of forming the p-type diffused regions 16 will now be described:

First, an insulating film 100 is formed over

(22)

the upper surface of the Si region 15. The insulating film 100 may be formed e.g. by thermal oxidization. The surface of the Si region 15 is oxidized so that the oxidized film 100 (i.e. a film of SiO_2) is formed by heating the Si substrate 11 supporting the Si region 15 in an atmosphere of wet O_2 at $1,000^\circ\text{C}$ for 110 mins. Next, in order to form four semiconductor resistor regions in the Si region 15 above the n^+ -type buried region 13a, the oxide film 100 is selectively removed by a wellknown technique such as photo-etching to expose parts of the n-type Si region 15. P-type impurities such as boron (B) ions are introduced into the exposed surfaces of the Si region 15 by predeposition or ion implantation, so that p-type diffused regions 16 of a depth of 2 to 3 μm and a sheet resistance of 100 ohm per square are formed by drive-in diffusion of the p-type impurities into the Si region 15. The predeposition is achieved by Si placing a solid impurity source of B_2O_3 together with the Si wafer in a quartz tube, keeping the interior of the quartz tube evacuated, and heating the quartz tube to about 900°C , thereby to deposit solid B_2O_3 over the surface of the Si wafer. If predeposition is used, after the drive-in diffusion, the boron glass covering the surfaces of the diffused regions 16 and the oxide film 100 is removed. Then, a thin oxide film 100a

23

- 9 -

is formed over the diffused regions 16 by oxidizing the exposed surfaces of the diffused regions 16.

5 If ion implantation is used, however, boron ions are implanted into the Si wafer at an implantation energy of 75 keV, and a dose of 1×10^{13} atoms/cm². In order to prevent the surface of the Si region 15 being damaged by the ions during ion implantation, it is preferable that the oxide film 100a is formed before ion implantation, and that the boron ions are
10 then introduced through the oxide film 100a into the Si region 15. The thin oxide film (100, 100a) is formed by the thermal oxidization.

STEP 6.

As shown in Figure 7, highly doped p⁺-type diffused
15 regions 17 (which will form electrode contacts) are formed so that they are connected to the terminals of the diffused gauge resistors 16. Simultaneously with the formation of the diffused regions 17, p⁺-type diffused regions 18 are formed so as to
20 contact the p-type buried isolation region 14a, and form an isolation region.

STEP 7.

As shown in Figure 8, n⁺-type regions 19, which form channel stoppers, are provided so as to enclose each
25 of the diffused regions (gauge resistors or piezo-resistive elements) 16. After that, the oxide film 100 is treated by contact photo-etching and aluminium

(Al) wirings 20 formed by aluminium vacuum evaporation and aluminium etching. The surface of the semiconductor substrate 11 on which the Al wiring 20 is formed is covered with a passivation film 21 (Figure 9) of plasma nitride or Phosphorus Silicate Glass (PSG). This passivation film preferably has a thickness of about 1.2 μm , and is formed to prevent contamination of the oxide film 100 by the surrounding atmosphere. It is desirable that plasma nitride is used because it provides a stable film. However, a laminated film in which a PSG film (of about 0.2 μm thickness) and a plasma nitride film (of about 1.1 μm thickness) are formed one over the other, can be used as the passivation film.

15 STEP 8.

In order to form the diaphragm, as shown in Figures 9 and 11, a photoresist mask 24 is formed over the p^+ -type region 12a in the peripheral portion of the reverse surface of the substrate, and the substrate is anisotropically etched in a selective manner by alkaline etchants, such as KOH, to form a recess 22 in the unmasked central portion of the substrate 11.

Due to the characteristics of anisotropic etching, the etching rate differs greatly according to different impurity concentrations in the semiconductor substrate. As illustrated in Figure 12, the etching rate v drops abruptly at a high impurity

concentration of about 10^{19} atoms/cm³. As a result, during this etching step, the central substrate portion which has a low impurity concentration is rapidly etched in the direction of the arrows, as shown by the broken lines in Figure 10, whereas the highly doped peripheral region 12a is hardly etched at all. Consequently, the etching follows the shape of the side surfaces of the diffused region 12a. Etching in the lateral direction of the substrate is thus restricted because of the formation of the diffused region 12a. This means that a circular recess 22 is created if the mask used when the diffused region 12a is formed has a circular pattern. When the etching reaches the highly doped n⁺-type buried region 13a, the etching rate drops abruptly so that a flat base is obtained in the recess as a result of the slowing down of the etching. Thus a diaphragm of a thickness of 25 to 30 μ m (substantially equal to that of the epitaxial region) is achieved.

Figure 13 is a plan view of a diaphragm pressure sensor formed by the embodiment of the method of the present invention described above. In Figure 13, a circle 22b indicated by a solid line is the shape of a thin film portion providing the diaphragm, and a circle 22a indicated by a broken line is the shape of the opening forming the recess, which opening is

- 12 -

in turn the shape of the mask used to form the highly doped region 12a on the back of the substrate 11. A passivation film 30 covers the principal plane of the substrate in such a manner that terminals (or bonding pads) 23 are exposed. This passivation film 30 may be a film of CVD SiO_2 or a polyimide resin.

As shown in Figure 13, the plurality of p-type diffused regions 16, forming gauge resistors (R_1 , R_2 , R_3 and R_4), are arranged at four places on the surface of the thin film portion, parallel to the direction of the axis $\langle 110 \rangle$, which has the highest piezo-resistive effect, and corresponding terminals are formed of highly doped p^+ -type regions 17, contacted by the aluminium wirings 20. The aluminium wirings 20 connect the gauge resistors R_1 , R_2 , R_3 and R_4 into a bridge network with peripheral terminals 23. Figure 14 is a section taken along the line A - A' of Figure 13. The n^+ -type regions 19 acting as channel stoppers in Figure 14 are omitted from Figure 13; they are each formed in an annular shape so as to enclose the p-type diffused regions 16 and the p^+ -type regions 17.

According to the embodiment of the present invention described above, the following effects may be obtained.

(1) A recess of any shape may be formed without any restrictions due to the crystal orientation of the

semiconductor substrate, by forming a local difference in impurity concentration in the semi-conductor substrate, and then selectively etching that portion of the substrate with a lower impurity concentration.

5 (2) When the recess is being etched, lateral etching is restricted by a highly doped semiconductor region of an impurity concentration of at least 10^{19} atoms/cm³. As a result, the shape of the recess is controlled and the shape of the diaphragm, particularly its size, is not changed by variations in etching
10 time.

(3) Because it is easy to form a circular recess in a semiconductor substrate, a silicon diaphragm with a circular recess can be formed.

15 (4) Irregularities in strains due to the shape of the periphery of the diaphragm can be eliminated by adopting a circular diaphragm in a diaphragm pressure sensor so that the temperature characteristics of the diffused gauge resistors can be improved.

20 Other embodiments of the present invention will now be described.

In a second embodiment, step 6 may be carried out before step 5. In this case, the diffused regions 16 forming the gauge resistors are thermally
25 influenced by the formation of the other diffused regions 17 and 18. However, the diffused regions 16 must have very accurate resistances, so that it is

preferable that the diffused regions 16 are formed after all the other semiconductor regions have been formed.

5 In a third embodiment, to form a recess (or diaphragm) with a very accurately controlled shape, p-type impurities may be introduced in Step 1 of the first embodiment into both principal planes of the semiconductor substrate by drive-in diffusion, to form the p^+ -type region 12. This p^+ -type region 12
10 has shape indicated by the broken lines on Figure 15. The p^+ -type region 12 restrains lateral etching. As a result, it is easy to form a recess (or diaphragm) of a predetermined shape, independent of variation in the etching time.

15 In a fourth embodiment it is possible to provide a semiconductor integrated circuit device in which a pressure sensor and a peripheral circuit (e.g., a temperature-compensating circuit or an amplifier circuit) required by the pressure sensor are built
20 into a single semiconductor substrate. The peripheral circuit has at least one transistor (e.g. a bipolar transistor, or an insulated gate field effect transistor). For example, a bipolar type transistor can be formed in one n-type isolated
25 region which is enclosed by the isolation region (the p^+ -type region 18 of Figure 7).

In a fifth embodiment N-type impurities may be

introduced in the step (2) of the first embodiment to form an n^+ -type buried region 13a (shown in Figure 5). This step, i.e., the formation of the n^+ -type buried region 13a is important for accurate control of the thickness of the diaphragm. However, that step is not essential when the diaphragm is formed by anisotropic etching.

A pressure sensor fabricated by the method of the present invention can be applied to a pressure-measuring device for an automotive engine, an oil pressure measuring device, or a clinical sphygmomanometer.

CLAIMS:

1. A method of fabricating a semiconductor pressure sensor having a predetermined diaphragm configuration, comprising the steps of:

5 forming a highly doped region in a single crystal semiconductor substrate with first and second principal planes facing each other by covering a part of the first principal plane by a mask for defining the predetermined diaphragm configuration, and selectively introducing
10 impurities into a part of the substrate which is not covered by the mask;

forming an epitaxial semiconductor region on the second principal plane;

forming semiconductor regions for gauge resistors by
15 selectively introducing impurities into the epitaxial semiconductor region; and

etching a part of the first principal plane other than that in which the highly doped region is formed, using the highly doped region as an etching stop thereby to form the
20 predetermined diaphragm configuration such that it is bounded by the highly doped region, whereby a controlled recess providing the predetermined diaphragm configuration, independent of the crystal orientation of the semiconductor substrate, is formed.

2. A method of fabricating a semiconductor device
25 according to claim 1, wherein the semiconductor substrate is a crystalline silicon substrate of which the principal plane thereof is positioned in or adjacent to the (100) plane thereof.



21

- 17 -

3. A method of fabricating a semiconductor device according to claim 1 or claim 2, wherein the etching step is conducted by anisotropic etching using alkaline etchants.

5 4. The method of fabricating a semiconductor device according to any one of the preceding claims, wherein the highly doped region has an impurity concentration of at least 10^{19} atoms/cm³.

5. A method of fabricating a semiconductor device
10 substantially as any one herein described with reference to and as illustrated in the accompanying drawings.



* C L M S *