CLAIMS

1. A computer program product for providing an interrupt signal to a guest operating system executed using one or more processors of a plurality of processors of a computer system assigned for usage by the guest operating system, the computer program product comprising: at least one computer readable storage medium readable by at least one processing circuit and storing instructions for performing a method comprising: receiving, by a bus attachment device from a bus connected module of a plurality of bus connected modules operationally coupled to the plurality of processors via the bus attachment device, an interrupt signal with an interrupt target ID, the interrupt target ID identifying one processor of the plurality of processors assigned for usage by the guest operating system as a target processor to handle the interrupt signal; selecting, by the bus attachment device, a directed interrupt signal vector assigned to the interrupt target ID to which the interrupt signal is addressed; selecting, by the bus attachment device in the directed interrupt signal vector, a directed interrupt signal indicator assigned to the bus connected module which issued the interrupt signal; updating, by the bus attachment device, the directed interrupt signal indicator such that the directed interrupt signal indicator indicates that there is the interrupt signal issued by the bus connected module and addressed to the interrupt target ID to be handled; and forwarding, by the bus attachment device, the interrupt signal to the target processor.

2. The computer program product of claim 1, wherein the computer system further comprises a memory, the memory comprising a respective directed interrupt signal vector per interrupt target ID, each directed interrupt signal vector comprising a respective directed interrupt signal indicator per bus connected module, and each directed interrupt signal vector indicating whether there is a respective interrupt signal issued by the respective bus connected module and addressed to the respective interrupt target ID to be handled, and wherein each directed interrupt signal indicator assigned to the same bus connected module comprises a same offset within the respective directed interrupt signal vector comprising the respective interrupt signal indicator.

3. The computer program product of claim 1, wherein the method further comprises: retrieving, by the bus attachment device, a copy of an interrupt table entry assigned to the interrupt target ID from an interrupt table, the copy of the interrupt table entry comprising a directed interrupt signal vector address indicator indicating a memory address of the directed interrupt signal vector assigned to the interrupt target ID to which the interrupt signal is addressed; and using, by the bus attachment device, the memory address of the directed interrupt signal vector to select the directed interrupt signal vector assigned to the interrupt target ID to which the interrupt signal is addressed.

4. The computer program product of claim 3, wherein the method further comprises: retrieving, by the bus attachment device, a copy of a device table entry from a device table, the copy of the device table entry comprising an interrupt table address indicator indicating a memory address of the interrupt table; and using, by the bus attachment device, the memory address of the interrupt table to retrieve the copy of the interrupt table entry.

5. The computer program product of claim 4, wherein the copy of the device table entry further comprises a directed interrupt signal offset indicator indicating an offset of the directed interrupt signal indicator assigned to the bus connected module which issued the interrupt signal.

6. The computer program product of claim 1, wherein the method further comprises: selecting, by the bus attachment device from a directed interrupt summary vector, a directed interrupt summary indicator assigned to the interrupt target ID to which the interrupt signal is addressed; and updating, by the bus attachment device, the directed interrupt summary indicator such that the directed interrupt summary indicator indicates that there is the interrupt signal addressed to the interrupt target ID to be handled.

7. The computer program product of claim 6, wherein the method further comprises: retrieving, by the bus attachment device, a copy of an interrupt table entry assigned to the interrupt target

ID, the copy of the interrupt table entry comprising a directed interrupt summary vector address indicator indicating a memory address of the directed interrupt summary vector; and using, by the bus attachment device, the memory address of the directed interrupt summary vector to select the directed interrupt summary indicator assigned to the interrupt target ID to which the interrupt signal is addressed.

8. The computer program product of claim 7, wherein the copy of the interrupt table entry further comprises a directed interrupt summary offset indicator indicating an offset of the directed interrupt summary indicator assigned to the interrupt target ID within the directed interrupt summary vector.

9. The computer program product of claim 1, wherein the method further comprises: translating, by the bus attachment device, the interrupt target ID of the target processor received with the interrupt signal to a logical processor ID of the target processor; and using the logical processor ID of the target processor to address the target processor as a target of the interrupt signal, when forwarding the interrupt signal to the target processor.

10. The computer program product of claim 9, wherein the method further comprises: retrieving, by the bus attachment device, a copy of an interrupt table entry assigned to the interrupt target ID from an interrupt table, the copy of the interrupt table entry comprising a current mapping of the interrupt target ID to the logical processor ID; and using, by the bus attachment device, the current mapping to translate the interrupt target ID to the logical processor ID.

11. The computer program product of claim 1, wherein the method further comprises: checking, by the bus attachment device, a direct signaling indicator indicating whether the target processor is to be addressed directly; performing the forwarding, based on the direct signaling indicator indicating a direct forwarding of the interrupt signal, wherein the forwarding uses a logical processor ID of the target processor to address the target processor directly; and forwarding the

interrupt signal using broadcasting, based on the direct signaling indicator not indicating the target processor is to be addressed directly.

12. The computer program product of claim 1, wherein the method further comprises: checking, by the bus attachment device, a copy of a running indicator indicating whether the target processor identified by the interrupt target ID is scheduled for usage by the guest operating system; performing the forwarding, based on the target processor being scheduled for usage by the guest operating system, the forwarding comprising forwarding the interrupt signal using a logical processor ID of the target processor to address the target processor directly; and forwarding the interrupt signal for handling using broadcasting, based on the target processor not being scheduled for usage by the guest operating system.

13. The computer program product of claim 1, wherein the method further comprises: checking, by the bus attachment device, an interrupt blocking indicator indicating whether the target processor identified by the interrupt target ID is currently blocked from receiving interrupt signals; performing the forwarding, based on the target processor not being blocked from receiving interrupt signals, the forwarding comprising forwarding the interrupt signal using a logical processor ID of the target processor to address the target processor directly; and forwarding the interrupt signal using broadcasting, based on the target processor being blocked from receiving interrupt signals.

14. A computer system for providing an interrupt signal to a guest operating system executed using one or more processors of a plurality of processors of a computer system assigned for usage by the guest operating system, the computer system configured to perform a method, said method comprising: receiving, by a bus attachment device from a bus connected module of a plurality of bus connected modules operationally coupled to the plurality of processors via the bus attachment device, an interrupt signal with an interrupt target ID, the interrupt target ID identifying one processor of the plurality of processors assigned for usage by the guest operating system as a target processor to handle the interrupt signal; selecting, by the bus attachment

device, a directed interrupt signal vector assigned to the interrupt target ID to which the interrupt signal is addressed; selecting, by the bus attachment device in the directed interrupt signal vector, a directed interrupt signal indicator assigned to the bus connected module which issued the interrupt signal; updating, by the bus attachment device, the directed interrupt signal indicator such that the directed interrupt signal indicator indicates that there is the interrupt signal issued by the bus connected module and addressed to the interrupt target ID to be handled; and forwarding, by the bus attachment device, the interrupt signal to the target processor.

15. The computer system of claim 14, wherein the method further comprises: retrieving, by the bus attachment device, a copy of an interrupt table entry assigned to the interrupt target ID from an interrupt table, the copy of the interrupt table entry comprising a directed interrupt signal vector address indicator indicating a memory address of the directed interrupt signal vector assigned to the interrupt target ID to which the interrupt signal is addressed; and using, by the bus attachment device, the memory address of the directed interrupt signal vector to select the directed interrupt signal vector assigned to the interrupt target ID to which the interrupt signal is addressed.

16. The computer system of claim 14, wherein the method further comprises: translating, by the bus attachment device, the interrupt target ID of the target processor received with the interrupt signal to a logical processor ID of the target processor; and using the logical processor ID of the target processor to address the target processor as a target of the interrupt signal, when forwarding the interrupt signal to the target processor.

17. The computer system of claim 16, wherein the method further comprises: retrieving, by the bus attachment device, a copy of an interrupt table entry assigned to the interrupt target ID from an interrupt table, the copy of the interrupt table entry comprising a current mapping of the interrupt target ID to the logical processor ID; and using, by the bus attachment device, the current mapping to translate the interrupt target ID to the logical processor ID.

18. A computer-implemented method of providing an interrupt signal to a guest operating system executed using one or more processors of a plurality of processors of a computer system assigned for usage by the guest operating system, the computer-implemented method comprising: receiving, by a bus attachment device from a bus connected module of a plurality of bus connected modules operationally coupled to the plurality of processors via the bus attachment device, an interrupt signal with an interrupt target ID, the interrupt target ID identifying one processor of the plurality of processors assigned for usage by the guest operating system as a target processor to handle the interrupt signal; selecting, by the bus attachment device, a directed interrupt signal vector assigned to the interrupt target ID to which the interrupt signal is addressed; selecting, by the bus attachment device in the directed interrupt signal vector, a directed interrupt signal indicator assigned to the bus connected module which issued the interrupt signal; updating, by the bus attachment device, the directed interrupt signal indicator such that the directed interrupt signal indicator indicates that there is the interrupt signal issued by the bus connected module and addressed to the interrupt target ID to be handled; and forwarding, by the bus attachment device, the interrupt signal to the target processor.

19. The computer-implemented method of claim 18, further comprising: retrieving, by the bus attachment device, a copy of an interrupt table entry assigned to the interrupt target ID from an interrupt table, the copy of the interrupt table entry comprising a directed interrupt signal vector address indicator indicating a memory address of the directed interrupt signal vector assigned to the interrupt target ID to which the interrupt signal is addressed; and using, by the bus attachment device, the memory address of the directed interrupt signal vector to select the directed interrupt signal vector assigned to the interrupt target ID to which the interrupt signal is addressed.

20. The computer-implemented method of claim 18, further comprising: translating, by the bus attachment device, the interrupt target ID of the target processor received with the interrupt signal to a logical processor ID of the target processor; and using the logical processor ID of the target processor to address the target processor as a target of the interrupt signal, when forwarding the interrupt signal to the target processor.