Description

Background of the Invention

This invention relates to semiconductor integrated circuits and more particularly to methods for processing dielectrically isolated devices in such circuits.

A commonly used method for processing metal oxide semiconductor (MOS) transistors and bipolar transistors in integrated circuits at a major surface of a semiconductive silicon body (substrate) involves the local oxidation of silicon (LOCOS) process for electrically isolating neighboring transistors. In that process, the major surface of the silicon substrate is masked with a silicon nitride layer having (rectangular) window areas, and the exposed silicon in these window areas is oxidized. However, owing to lateral oxidation of silicon under the silicon nitride mask, the LOCOS process undesirably increases the required distance between neighboring transistors, whereby the transistor packing density is undesirably reduced.

In order to avoid the aforementioned disadvantage of the LOCOS process, selective epitaxial growth (SEG) of silicon has been proposed as an alternative. In SEG, an epitaxial layer of semiconductive silicon is grown on the exposed portions of the major surface of a semiconductive silicon body, these exposed portions being located at the bottom of windows in an insulating layer located on the major surface of the silicon body. At the same time, no silicon accumulates on the insulating layer--hence the use of the word "selective" in SEG. However, in prior art a major problem associated with SEG is the unwanted formation of facets at the corners of the windows, whereby significant portions of the overall resulting surface of the SEG silicon become undesirably non-planar, so that the transistor packing density again is reduced. For example, when fabricating an MOS transistor on a major surface of SEG silicon grown on silicon which is oriented (100), the undesired facets are oriented (311), these facets being undesired because it is desirable that the active region of the gate of the transistor everywhere be confined to areas overlying the portion of the major surface oriented (100).

In U.S. Patent No. 4,786,615 entitled "Method for Improved Surface Planarity in Selective Epitaxial Silicon," issued to Liaw et al on November 22, 1988, a method for SEG of silicon by chemical vapor deposition (into an assumedly rectangular window) was disclosed, in order to obtain a substantially planar epitaxial silicon surface. In that method, superimposed epitaxial silicon layers were grown in windows penetrating through a masking layer at temperatures above and below a transition point. The masking layer could be a single layer of insulating material, such as silicon dioxide, or it could be a multilayered mask, such as silicon dioxide located on doped polysilicon located on silicon dioxide. That method, however, requires careful control over temperature vs. time, which can be disadvantageous.

Accordingly, it would be desirable to have a method for SEG of semiconductive silicon or other semiconductor, which does not suffer from the disadvantage of prior art.

Summary of the Invention

In accordance with the invention we provide a selectively epitaxially grown semiconductor region and a method for making it as set forth in claim 1 and 7, respectively. It is advantageous that in addition the region have the features recited in claim 2. It is further advantageous that the region also have the features recited in claims 3 or 4. It is also advantageous that in addition the region have the features recited in claim 5. It is also advantageous that in addition the device have the features recited in claim 6. It is also advantageous that in addition the method have the features recited in claim 8. And it is advantageous that in addition the method have the features recited in claim 9.

Brief Description of the Drawing(s)

FIG. 1 is a top view diagram of a portion of an MOS transistor fabricated in a decorated window in SEG silicon, in accordance with a specific embodiment of the invention; and

FIG. 2 is a top view diagram of a portion of an MOS transistor fabricated in a decorated window in SEG silicon, in accordance with another specific embodiment of the invention;

FIG. 3 is a side elevational view of a cross section of the MOS transistor shown in FIG. 1 or FIG. 2;

FIG. 4 is a top view diagram of a decorated portion of a decorated window in accordance with another specific embodiment of the invention; and

FIG. 5 is a top view diagram of a decorated portion of a decorated window in accordance with yet another specific embodiment of the invention.

Detailed Description

Turning to the drawings, FIG. 1 shows a top view of a portion of an MOS transistor 300 in an intermediate stage of its fabrication. A relatively thick (typically about 800 nm) masking layer of silicon dioxide (field oxide) 202 has a top surface 105. This field oxide layer 202 is located on a major surface 201 (FIG. 3) of a monocrystalline silicon substrate 200 oriented (100). A decorated rectangular window, with major side edges 101 and 102 bounding its undecorated portion, has been cut through the thick field oxide 202; and an SEG silicon region 103, having a top major surface 104, has been formed in this decorated window. The major side edge 101 of the window runs parallel to the <100> crystallographic direction of the silicon substrate 200. Source and drain diffusion regions 205 and 206, respectively, are located in the SEG silicon region 103 at its major surface 104. A portion of

a gate electrode 204 is located on the top surface of a gate oxide layer 203 and has a width equal to w, the minimum feature size of the lithography being used to fabricate the transistor 300; and this gate electrode 204 typically extends from regions overlying the relatively thin gate oxide layer 203 into regions overlying the relatively thick field oxide 202.

Upon the gate oxide layer 203 is located a P-glass insulating layer 207. Rectangular apertures 208 and 209 through the resulting double oxide layer, composed of this P-glass layer and the gate oxide layer, typically have widths equal to w and enable the attachment of electrode contacts (not shown) to the source and drain regions 205 and 206, respectively, as known in the art. Advantageously, the top surface 104 of the SEG region 103 is located at a level that is below the top surface 105 of the field oxide 202, in order to suppress sidewall inversion of, and hence to suppress parasitic transistors formed by, the SEG silicon underlying the gate electrode at places where the latter steps from regions overlying the gate oxide 203 to regions overlying the field oxide 202.

Turning now to FIG. 2, elements in FIG. 2 that are similar to those used in FIG. 1 are given the same reference numerals. Here in FIG. 2, again the side edge 101 is parallel to the <100> direction in the silicon substrate. However, each of the projections has three side edges, instead of four as in FIG. 1. The side edges AB and CD (in FIG. 2) are parallel to the <110> crystallographic direction in the silicon substrate. Advantageously, to minimize the additional area consumed by the projections AB=BC=CD=DA=w. A simple calculation shows that the additional area required for the projections shown in FIG. 2 is less than that required for the projections shown in FIG. 1.

It should be recognized that all fabrication steps for making the transistor are known in the art, except perhaps for the growth parameters to be used in the SEG step to form the region 103. For example, to form the SEG region 103 in windows (FIG. 2) the field oxide 202, first the silicon substrate was subjected to a five-minute pre-baking at about 1045 degrees C in a radiantly heated barrel chamber at a reduced pressure of about 53 mbar. Then the temperature was lowered to about 950 degrees C for the deposition cycle, with a deposition rate of approximately 0.07 μm per minute in the barrel chamber. The SEG process (of undoped silicon) was then achieved with a chemistry of SiH_2Cl_2, HCl, and H_2 at the reduced pressure of about 53 mbar and a mole ratio of HCl to SiH_2Cl_2 of 1.0 to 0.6. Doped SEG can be obtained by adding dopants to the ambient.

The pre-baking at 1045 degrees C reduces the native SiO_2 film on the silicon surface as well as any other oxide films formed during the chemical cleaning of the surface prior to the SEG process. Lowering the temperature at which SEG is performed to 950 degrees C is a compromise between good quality SEG and reasonably high growth rates. Use of the somewhat high HCl to SiH_2Cl_2 ratio (of 1.0 to 0.6) enhances the selectivity of growth favoring exposed silicon surfaces as opposed to exposed SiO_2 surfaces.

Instead of the projections having straight boundary edges as shown in FIGS. 1 and 2, they can advantageously have curvilinear boundary edges (lobes), in order to minimize further the required added surface area, as shown in FIGS. 4 and 5, respectively. Here in FIG. 4, the edges 101 and 102 of the original rectangular window intersect at point O, which is the center of a circular arc 124. This arc 124 subtends an angle of $3\pi/2$ radian; and the distance AE=w, just as in FIG. 1. The radius of this circular arc 124 is equal to $OE=AE/\sqrt{2} = w/\sqrt{2}$.

In FIG. 5, the edges 101 and 102 intersect at a point X which lies on a circular arc 125 centered at point O. In turn, point O lies along AD=w, the radius OA=OD=OX of this arc being equal to w/2.

In FIGS. 1 and 4 the distances across the mouths AE of the lobes are both equal to w; and in FIGS. 2 and 5 the distances across the mouths AD of the lobes are also both equal to w.

Other orientations of the surface of the silicon and other semiconductors can be used, as well as other shapes of the projections or lobes.

Claims

1. An integrated circuit comprising a selectively epitaxially grown semiconductor region located in a window in a masking layer, the window having a corner defined by an intersection of a first and a second edge of the window, the semiconductor region and the masking layer being located on a major surface of a monocrystalline semiconductor body, CHARACTERIZED IN THAT the corner of the window is provided with a projection, the window with the projection penetrating through the masking layer to the major surface of the semiconductor body, whereby the epitaxially grown semiconductor region is provided in the complete said window with said projection.

2. The circuit of claim 1 FURTHER CHARACTERIZED IN THAT the projection has at least a first edge running parallel to a crystallographic direction of the semiconductor body and has two other edges running perpendicular to the first edge.

3. The circuit of claim 2 FURTHER CHARACTERIZED IN THAT the projection has a total of only three edges.

4. The circuit of claim 2 FURTHER CHARACTERIZED IN THAT the projection has two edges running parallel to the crystallographic direction in addition to the two other edges running perpendicular to the first edge, for a total of four edges.

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a gate electrode 204 is located on the top surface of a gate oxide layer 203 and has a width equal to w, the minimum feature size of the lithography being used to fabricate the transistor 300; and this gate electrode 204 typically extends from regions overlying the relatively thin gate oxide layer 203 into regions overlying the relatively thick field oxide 202.

Upon the gate oxide layer 203 is located a P-glass insulating layer 207. Rectangular apertures 208 and 209 through the resulting double oxide layer, composed of this P-glass layer and the gate oxide layer, typically have widths equal to w and enable the attachment of electrode contacts (not shown) to the source and drain regions 205 and 206, respectively, as known in the art. Advantageously, the top surface 104 of the SEG region 103 is located at a level that is below the top surface 105 of the field oxide 202, in order to suppress sidewall inversion of, and hence to suppress parasitic transistors formed by, the SEG silicon underlying the gate electrode at places where the latter steps from regions overlying the gate oxide 203 to regions overlying the field oxide 202.

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In FIG. 5, the edges 101 and 102 intersect at a point X which lies on a circular arc 125 centered at point O. In turn, point O lies along AD=w, the radius OA=OD=OX of this arc being equal to w/2.

In FIGS. 1 and 4 the distances across the mouths AE of the lobes are both equal to w; and in FIGS. 2 and 5 the distances across the mouths AD of the lobes are also both equal to w.

Other orientations of the surface of the silicon and other semiconductors can be used, as well as other shapes of the projections or lobes.

Claims

1. An integrated circuit comprising a selectively epitaxially grown semiconductor region located in a window in a masking layer, the window having a corner defined by an intersection of a first and a second edge of the window, the semiconductor region and the masking layer being located on a major surface of a monocrystalline semiconductor body, CHARACTERIZED IN THAT the corner of the window is provided with a projection, the window with the projection penetrating through the masking layer to the major surface of the semiconductor body, whereby the epitaxially grown semiconductor region is provided in the complete said window with said projection.

2. The circuit of claim 1 FURTHER CHARACTERIZED IN THAT the projection has at least a first edge running parallel to a crystallographic direction of the semiconductor body and has two other edges running perpendicular to the first edge.

3. The circuit of claim 2 FURTHER CHARACTERIZED IN THAT the projection has a total of only three edges.

4. The circuit of claim 2 FURTHER CHARACTERIZED IN THAT the projection has two edges running parallel to the crystallographic direction in addition to the two other edges running perpendicular to the first edge, for a total of four edges.

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5. The integrated circuit of claim 1 comprising a transistor having a minimum feature size, the transistor being located within the semiconductor region, FURTHER CHARACTERIZED IN THAT the distance across the mouth of the projection is at least approximately equal to the minimum feature size.

6. The integrated circuit according to claim 5, FURTHER CHARACTERIZED IN THAT the transistor is an MOS transistor having a gate electrode, and the minimum feature size is the width of the gate electrode.

7. A process of selective epitaxial growth of a semiconductor region comprises the steps of

   (a) forming a window with a projection in a masking layer located on a major surface of a monocrystalline semiconductor body, the window having a corner defined by an intersection of first and second edges thereof, the projection being located at said corner, the window with the projection penetrating through the masking layer to the major surface of the semiconductor body; and
   (b) epitaxially growing semiconductor in said window with the projection.

8. The process of claim 7 in which the projection has at least a first edge running parallel to a crystallographic direction of the semiconductor body and has two other edges running perpendicular to the first edge.

9. The process of claim 7 or 8 in which step (b) is performed by means of a mixture of SiH_2Cl_2, HCl, and H_2.

Patentansprüche

1. Integrierte Schaltung, umfassend einen selektiv epitaxial aufgewachsenen, in einem Fenster in einer Maskierungsschicht angeordneten Halbleiterbereich, wobei das Fenster eine durch den Schnitt einer ersten und einer zweiten Kante des Fensters definierte Ecke hat, wobei der Halbleiterbereich und die Maskierungsschicht an eine Hauptoberfläche eines monokristallinen Halbleiterkörpers angeordnet sind,
   dadurch gekennzeichnet,
   daß die Ecke des Fensters mit einem Vorsprung versehen ist, wobei das Fenster mit dem Vorsprung durch die Maskierungsschicht zur Hauptoberfläche des Halbleiterkörpers dringt, wobei der epitaxial aufgewachsene Halbleiterbereich mit dem Vorsprung in dem vervollständigten Fenster bereitgestellt ist.

2. Schaltung nach Anspruch 1,
   ferner dadurch gekennzeichnet, daß der Vorsprung wenigstens eine erste Kante hat, die parallel zu einer kristallographischen Richtung des Halbleiterkörpers verläuft und zwei weitere Kanten hat, die senkrecht zur ersten Kante verlaufen.

3. Schaltung nach Anspruch 2,
   ferner dadurch gekennzeichnet, daß der Vorsprung insgesamt nur drei Kanten hat.

4. Schaltung nach Anspruch 2,
   ferner dadurch gekennzeichnet, daß zusätzlich zu den zwei senkrecht zur ersten Kante verlaufenden Kanten der Vorsprung zwei Kanten hat, die parallel zu der kristallographischen Richtung verlaufen, um insgesamt vier Kanten zu bilden.

5. Integrierte Schaltung nach Anspruch 1,
   umfassend einen Transistor mit einer minimalen Strukturgröße, wobei der Transistor innerhalb des Halbleiterbereichs angeordnet ist,
   ferner dadurch gekennzeichnet, daß die Strecke quer zum Mund des Vorsprungs wenigstens gleich der minimalen Strukturgröße ist.

6. Integrierte Schaltung nach Anspruch 5,
   ferner dadurch gekennzeichnet, daß der Transistor ein MOS-Transistor mit einer Gate-Elektrode ist und die minimale Strukturgröße die Breite der Gate-Elektrode ist.

7. Verfahren zum epitaxialen Aufwachsen eines Halbleiterbereichs umfassend die Schritte des:

   a) Ausbildens eines Fensters mit einem Vorsprung in einer Maskierungsschicht, die an einer Hauptoberfläche eines monokristallinen Halbleiterkörpers angeordnet ist, wobei das Fenster eine durch einen Schnitt einer seiner ersten und seiner zweiten Kante definiert ist, wobei der Vorsprung an der Ecke angeordnet ist, wobei das Fenster mit dem Vorsprung durch die Maskierungsschicht zur Hauptoberfläche des Halbleiterkörpers dringt und
   b) epitaxiales Aufwachsen eines Halbleiters in dem Fenster mit dem Vorsprung.

8. Verfahren nach Anspruch 7,
   bei welchem der Vorsprung wenigstens eine erste Kante hat, die parallel zu einer kristallographischen Richtung des Halbleiterkörpers verläuft und zwei andere Kanten hat, die senkrecht zur ersten Kante verlaufen.

9. Verfahren nach Anspruch 7 oder 8,
   bei welchem der Schritt b) mittels einer Mischung von SiH_2Cl_2, HCl und H_2 durchgeführt wird.

Revendications

1. Circuit intégré comprenant une région semi-conductrice formée par croissance épitaxiale sélective, située dans une fenêtre pratiquée dans une couche de masquage, la fenêtre ayant un angle défini par une intersection d'un premier et d'un second bords de la fenêtre, la région semi-conductrice et la couche de masquage étant situées sur une surface principale d'un corps semi-conducteur monocristallin, caractérisé en ce que l'angle de la fenêtre est muni d'une protubérance, la fenêtre munie de la protubérance pénétrant dans la couche de masquage jusqu'à la surface principale du corps semi-conducteur, de sorte que la région semi-conductrice formée par croissance épitaxiale soit réalisée dans la totalité de cette fenêtre munie de cette projection.

2. Circuit selon la revendication 1, caractérisé en outre en ce que la protubérance a au moins un premier bord s'étendant parallèlement à la direction cristallographique du corps semi-conducteur et a deux autres bords s'étendant perpendiculairement au premier bord.

3. Circuit selon la revendication 2, caractérisé en outre en ce que la protubérance a un total de seulement trois bords.

4. Circuit selon la revendication 2, caractérisé en ce que la protubérance a deux bords s'étendant parallèlement à la direction cristallographique en plus des deux autres bords qui s'étendent perpendiculairement au premier bord, pour un total de quatre bords.

5. Circuit intégré selon la revendication 1, comprenant un transistor ayant une taille de trait minimale, le transistor étant situé à l'intérieur de la région semi-conductrice, caractérisé en outre en ce que l'ouverture de la protubérance est au moins approximativement égale à la taille de trait minimale.

6. Circuit intégré selon la revendication 5, caractérisé en outre en ce que le transistor est un transistor MOS ayant une électrode de grille, et la taille de trait minimale est la largeur de l'électrode de grille.

7. Procédé de croissance épitaxiale sélective d'une région semi-conductrice comprenant les étapes qui consistent:

   (a) à former une fenêtre munie d'une protubérance dans une couche de masquage située sur une surface principale d'un corps semi-conducteur monocristallin, la fenêtre ayant un angle défini par une intersection entre des premier et second bords de celle-ci, la protubérance étant située à l'emplacement dudit angle, la fenêtre munie de la protubérance pénétrant dans la couche de masquage jusqu'à la surface principale du corps semi-conducteur; et
   (b) à faire croître par épitaxie un semi-conducteur dans la fenêtre munie de la protubérance.

8. Procédé selon la revendication 7, dans lequel la protubérance a au moins un premier bord s'étendant parallèlement à la direction cristallographique du corps semi-conducteur et a deux autres bords s'étendant perpendiculairement au premier bord.

9. Procédé selon la revendication 7 ou 8, dans lequel l'étape (b) est effectuée au moyen d'un mélange de SiH_2Cl_2, HCl, et H_2.