WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

first and second macroblocks arranged in a first direction; and

a plurality of cells between the first macroblock and the second macroblock, the plurality of cells including,

at least one first ending cell adjacent to the first macroblock, the at least one first ending cell having a first width in the first direction,

at least one second ending cell adjacent to the second macroblock, the at least one second ending cell having a second width different from the first width in the first direction, and

at least one standard cell between the at least one first ending cell and the at least one second ending cell, and

wherein only one of the at least one first ending cell and the at least one second ending cell comprises a tap configured to receive a power supply voltage or a ground voltage and provide the power supply voltage or the ground voltage to an active region.

2. The integrated circuit of claim 1, wherein the at least one first ending cell comprises:

a first active region;

the tap on the first active region; and

a first contact on the tap, the first contact extending in a second direction perpendicular to the first direction and electrically connected to a first power rail to which the power supply voltage is applied or a second power rail to which the ground voltage is applied.

3. The integrated circuit of claim 2, wherein the at least one first ending cell further comprises:

a second active region; and

a dummy contact on the second active region.

4. The integrated circuit of claim 2, wherein the at least one first ending cell further comprises:

first gate lines extending in the second direction and parallel to each other; and

a first blocking layer between the first macroblock and the first gate lines and extending in the second direction,

wherein a width of the first blocking layer in the first direction is greater than a width of each of the first gate lines in the first direction.

5. The integrated circuit of claim 2, wherein the at least one first ending cell further comprises:

a second contact adjacent to the first contact in the first direction, the second contact forming a capacitor with the first contact.

6. The integrated circuit of claim 2, wherein the at least one second ending cell comprises:

a third active region; and

a dummy contact on the third active region.

7. The integrated circuit of claim 6, wherein the at least one second ending cell further comprises:

second gate lines extending in the second direction and parallel to each other; and

a second blocking layer between the second macroblock and the second gate lines and extending in the second direction,

wherein a width of the second blocking layer in the first direction is greater than a width of each of the second gate lines in the first direction.

8. The integrated circuit of claim 1, wherein the first macroblock and the at least one first ending cell are spaced apart from each other by a first space in the first direction, and the second macroblock and the at least one second ending cell are spaced apart from each other by a second space in the first direction.

9. The integrated circuit of claim 1, wherein the first macroblock borders the at least one first ending cell in the first direction or the second macroblock borders the at least one second ending cell in the first direction.

10. The integrated circuit of claim 1, wherein the at least one first ending cell comprises a plurality of first ending cells arranged in a line in a second direction perpendicular

to the first direction, and the at least one second ending cell comprises a plurality of second ending cells arranged in a line in the second direction.

11. The integrated circuit of claim 1, further comprising:

a third macroblock adjacent to the second macroblock in a second direction perpendicular to the first direction,

wherein the plurality of cells further comprise at least one third ending cell adjacent the third macroblock and having the second width in the first direction.

12. The integrated circuit of claim 1, further comprising:

a third macroblock adjacent to the first macroblock in a second direction perpendicular to the first direction,

wherein the plurality of cells further comprise at least one third ending cell adjacent the third macroblock and having the first width in the first direction.

13. An integrated circuit comprising:

first and second macroblocks arranged in a first direction; and

a plurality of cells between the first macroblock and the second macroblock, the plurality of cells including,

first ending cells adjacent to the first macroblock, the first ending cells arranged in a line in a second direction perpendicular to the first direction, each of the first ending cells having a first width in the first direction,

second ending cells adjacent to the second macroblock, the second ending cells arranged in a line in the second direction, each of the second ending cells having the first width in the first direction, and

center cells arranged in a line in the second direction in an area between the first ending cells and the second ending cells, and

wherein each of the center cells comprises a tap configured to receive a power supply voltage or a ground voltage on an active region.

14. The integrated circuit of claim 13, wherein each of the center cells has a second width different from the first width in the first direction.

15. The integrated circuit of claim 13, wherein each of the first and second ending cells comprises:

an active region; and

a dummy contact on the active region.

16. The integrated circuit of claim 15, wherein

each of the first ending cells further comprises first gate lines extending in the second direction and parallel to each other, and a first blocking layer between the first macroblock and the first gate lines and extending in the second direction,

each of the second ending cells further comprises second gate lines extending in the second direction and parallel to each other, and a second blocking layer between the second macroblock and the second gate lines and extending in the second direction, and

a width of each of the first and second blocking layers in the first direction is greater than a width of each of the first and second gate lines in the first direction.

17. The integrated circuit of claim 13, wherein the first macroblock borders each of the first ending cells in the first direction or the second macroblock borders each of the second ending cells in the first direction.

18. A system-on-chip comprising:

an application processor including,

first and second macroblocks arranged in a first direction, and

a plurality of cells between the first and second macroblocks, the plurality of cells having,

first ending cells adjacent to the first macroblock and arranged in a line in a second direction perpendicular to the first direction, and

second ending cells arranged in a line in the second direction and being implemented asymmetrically to the first ending cells; and

a memory electrically connected to the application processor, and

wherein only one of the first ending cells or the second ending cells comprises a tap configured to receive a power supply voltage or a ground voltage and provide the power supply voltage or the ground voltage to an active region.