FIG. 1

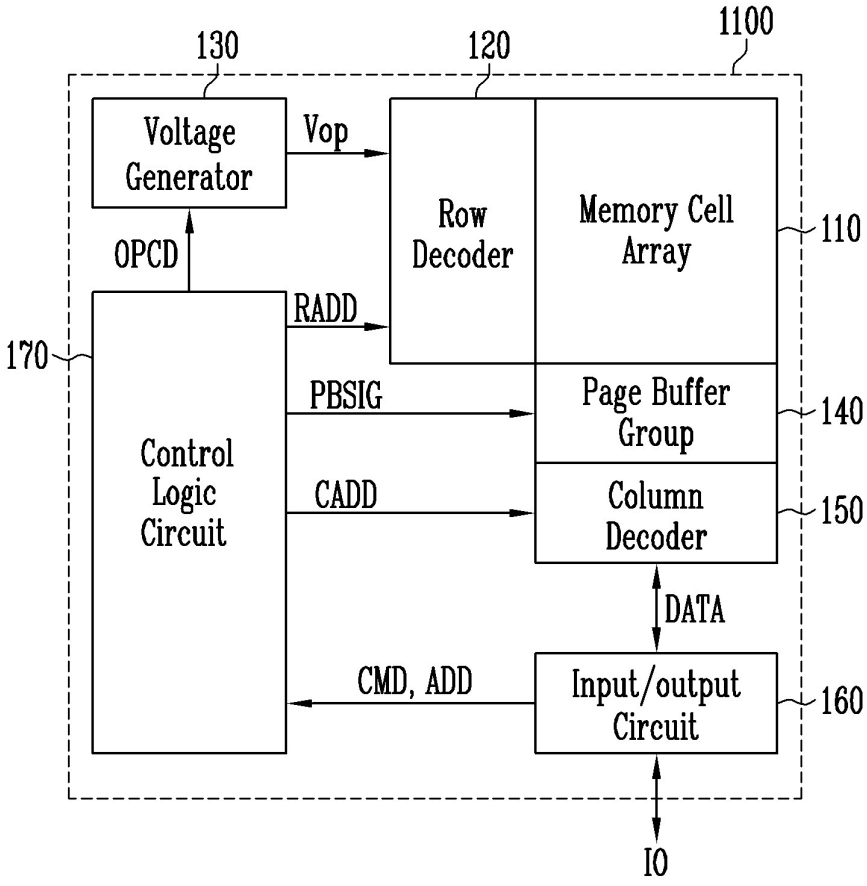

1100
130
120
Voltage Generator
Vop
Row Decoder
Memory Cell Array
110
OPCD
RADD
170
PBSIG
Page Buffer Group
140
Control Logic Circuit
CADD
Column Decoder
150
DATA
CMD, ADD
Input/output Circuit
160
IO

FIG. 2

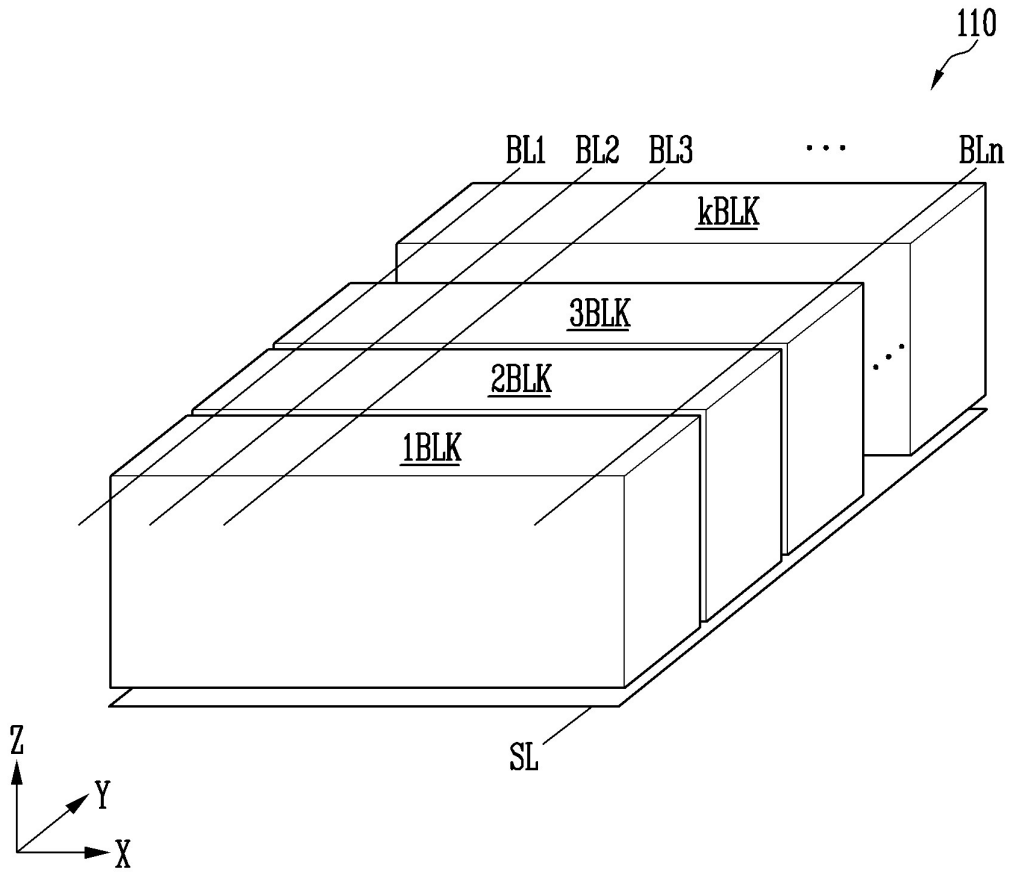


FIG. 3

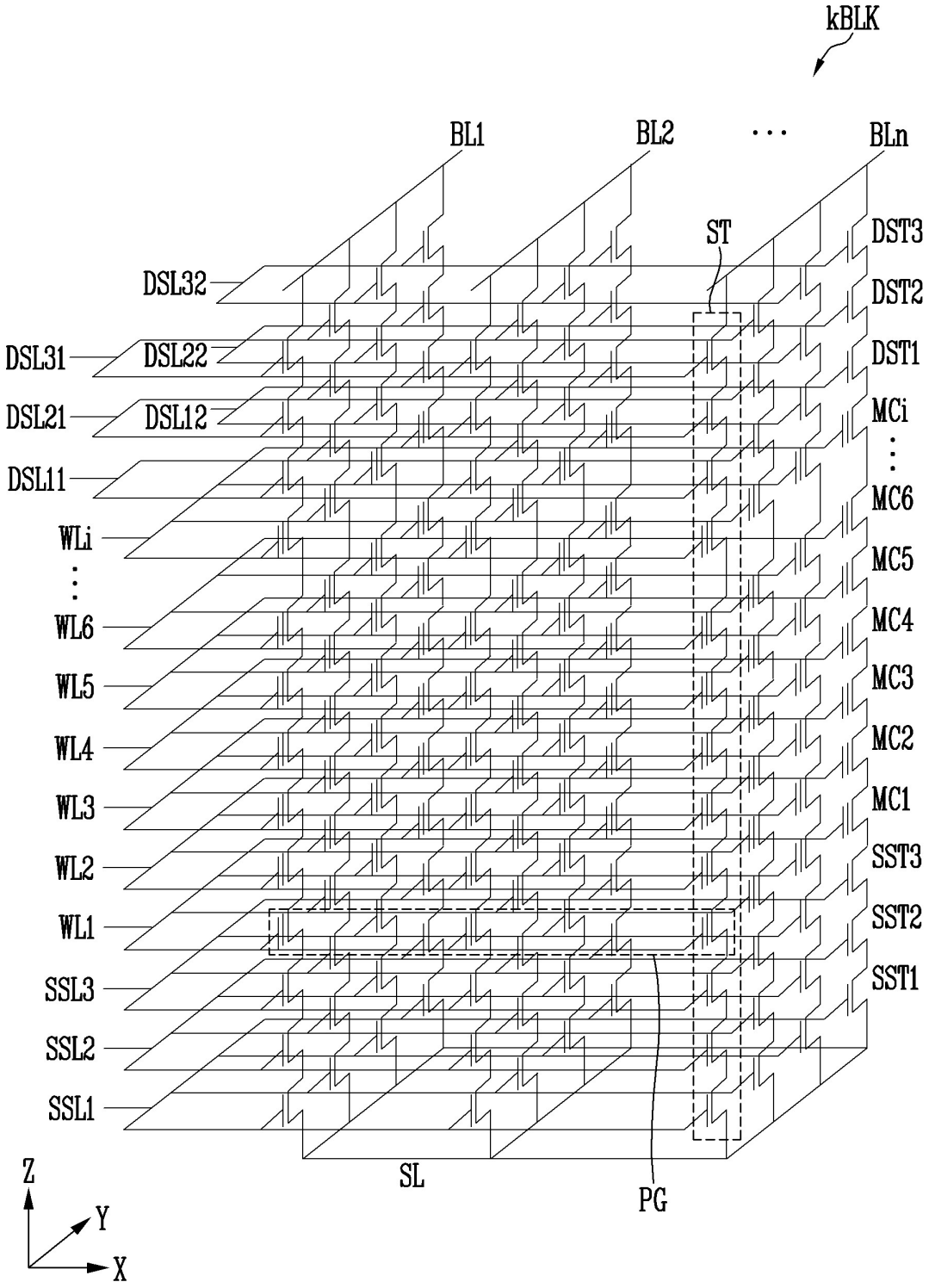

kBLK
BL1
BL2
BLn
ST
DST3
DST2
DST1
MCi
MC6
MC5
MC4
MC3
MC2
MC1
SST3
SST2
SST1
DSL32
DSL31
DSL22
DSL21
DSL12
DSL11
WLi
WL6
WL5
WL4
WL3
WL2
WL1
SSL3
SSL2
SSL1
SL
PG
Z
Y
X

FIG. 4

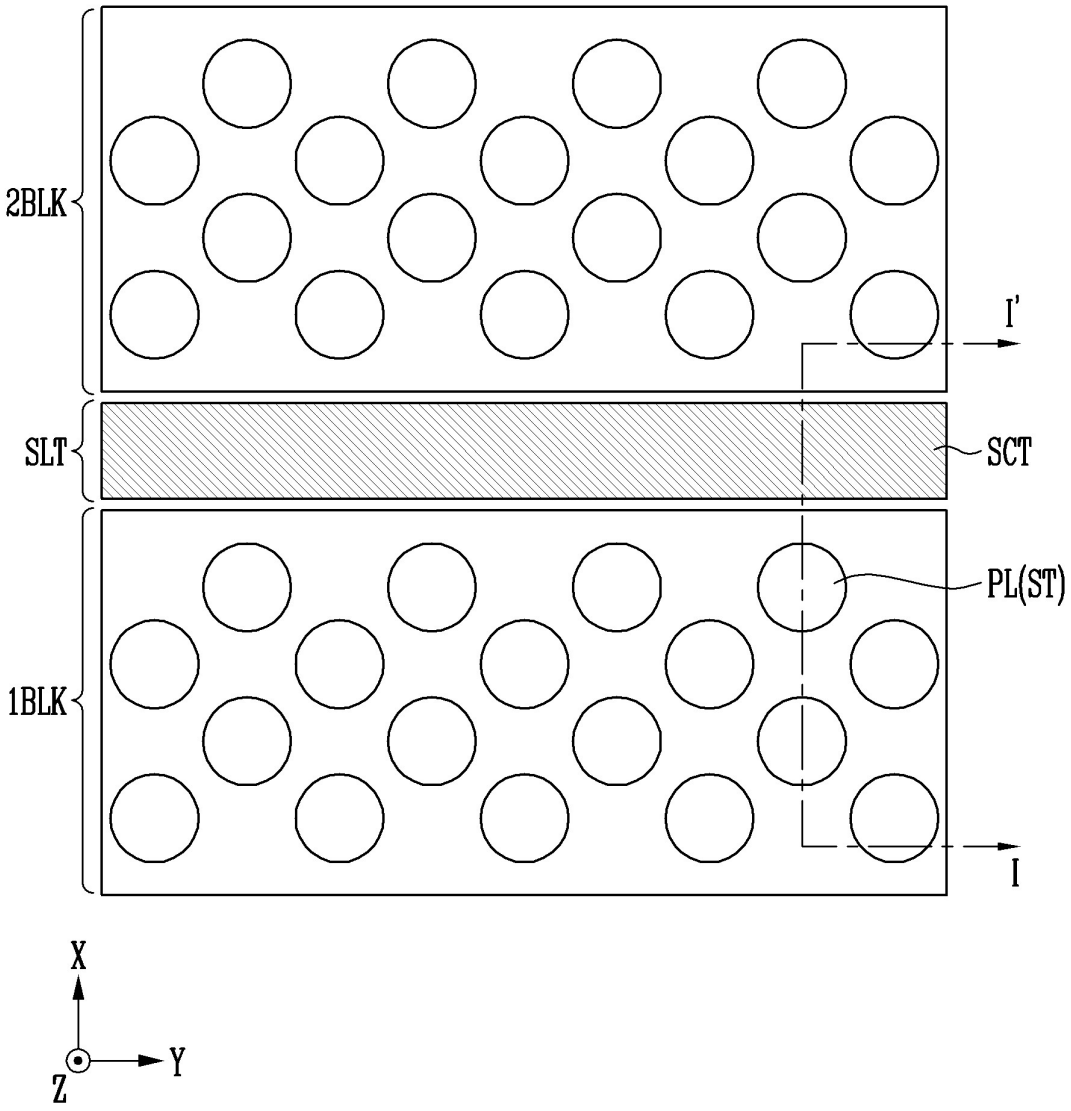


FIG. 5

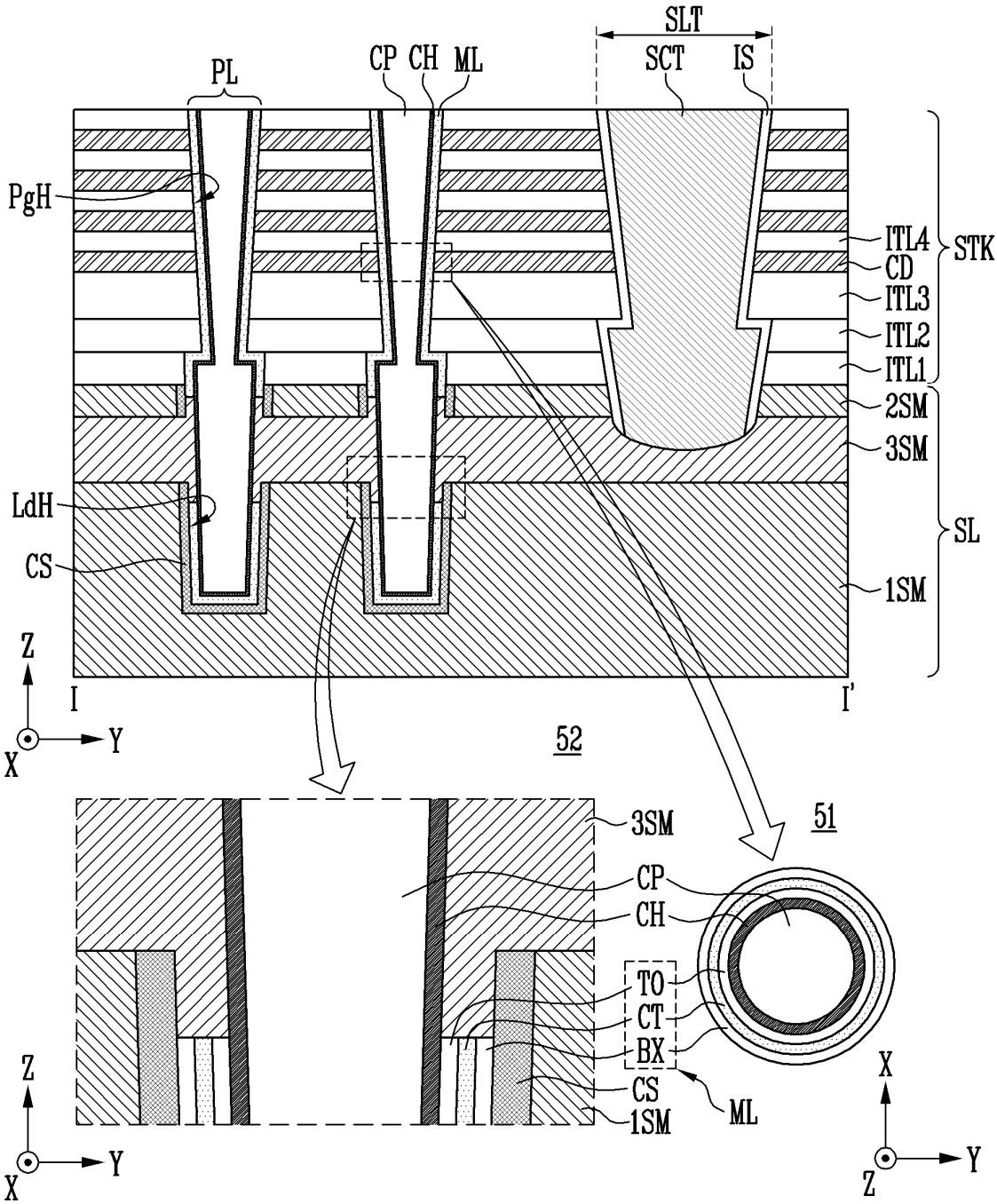

SLT
SCT
IS
PL
CP CH ML
PgH
ITL4
CD
ITL3
ITL2
ITL1
STK
2SM
3SM
SL
LdH
CS
1SM
Z
Y
X
I
I'
52
51
3SM
CP
CH
TO
CT
BX
CS
ML
1SM
Z
Y
X
X
Y
Z

FIG. 6A

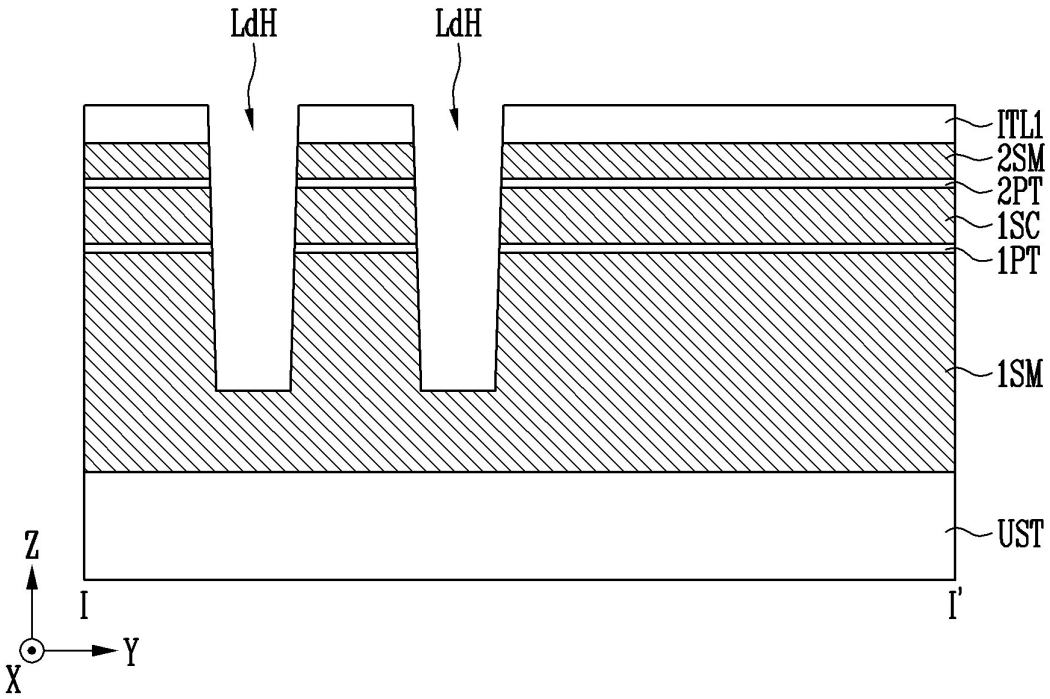


FIG. 6B

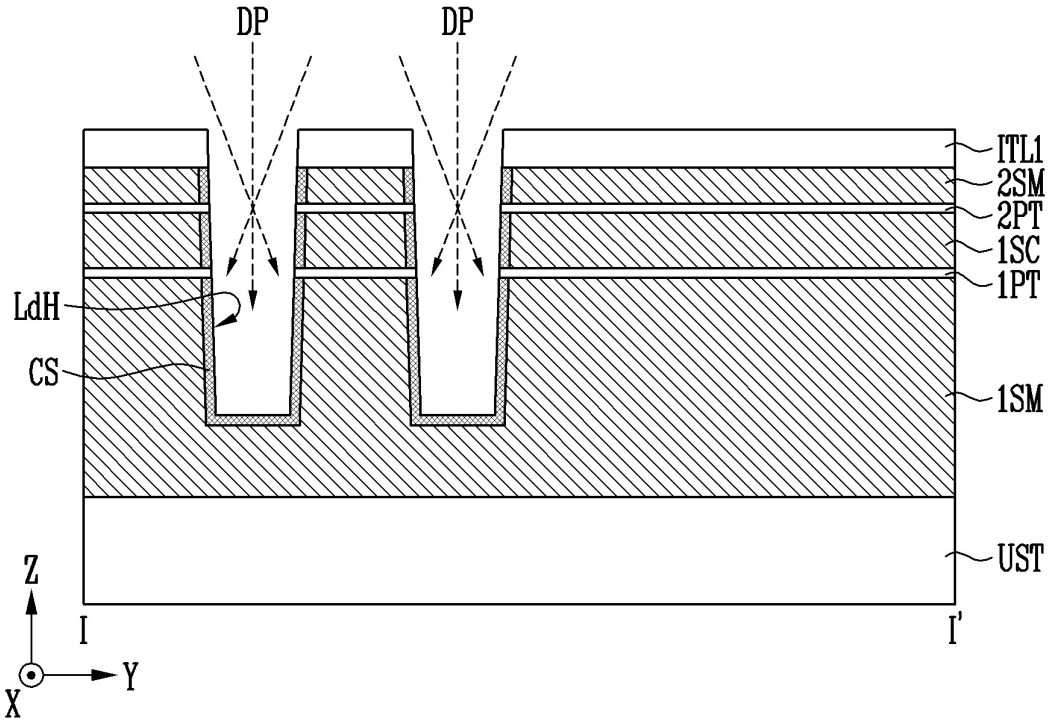


FIG. 6C

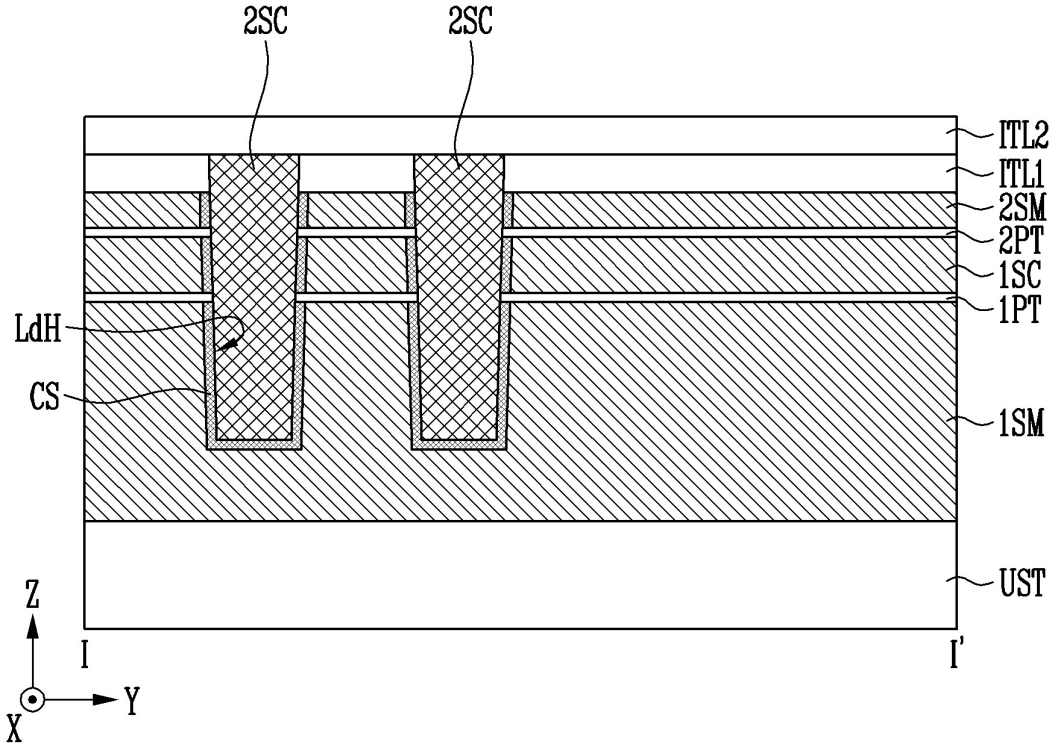


FIG. 6D

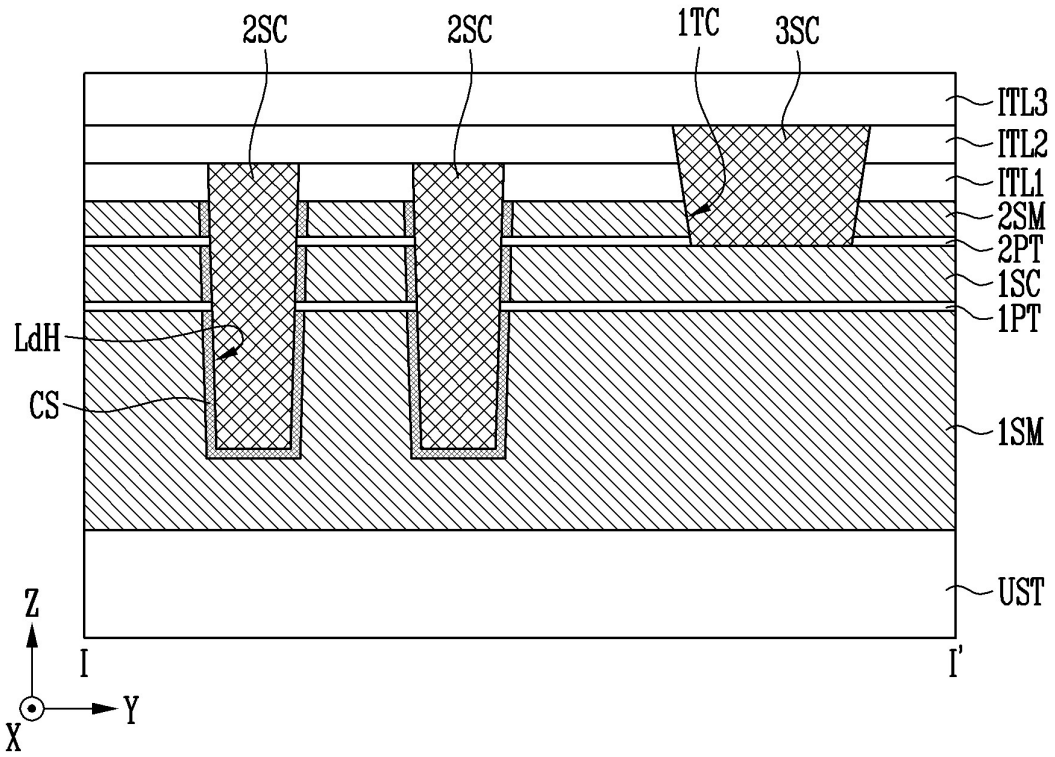

2SC
2SC
1TC
3SC
ITL3
ITL2
ITL1
2SM
2PT
1SC
1PT
LdH
CS
1SM
UST
Z
I
I'
Y
X

FIG. 6E

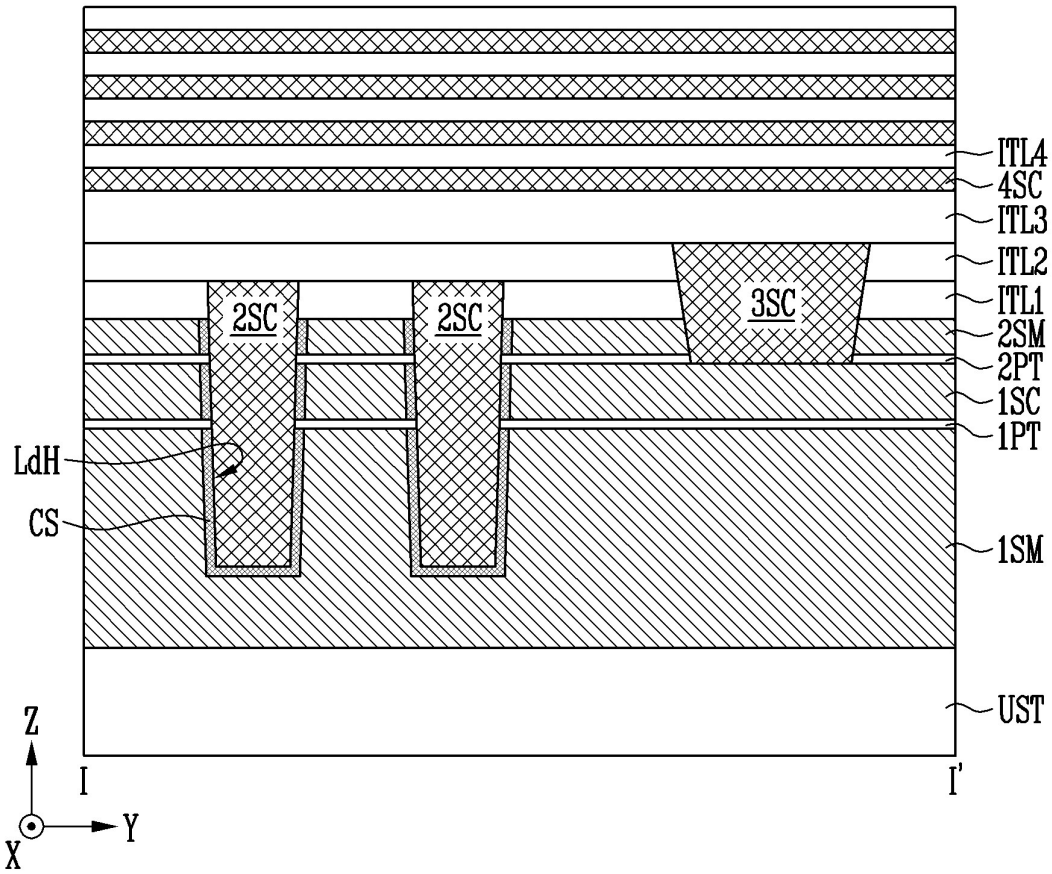

ITL4
4SC
ITL3
ITL2
ITL1
2SM
2PT
1SC
1PT
1SM
UST
2SC
2SC
3SC
LdH
CS
Z
Y
X
I
I'

FIG. 6F

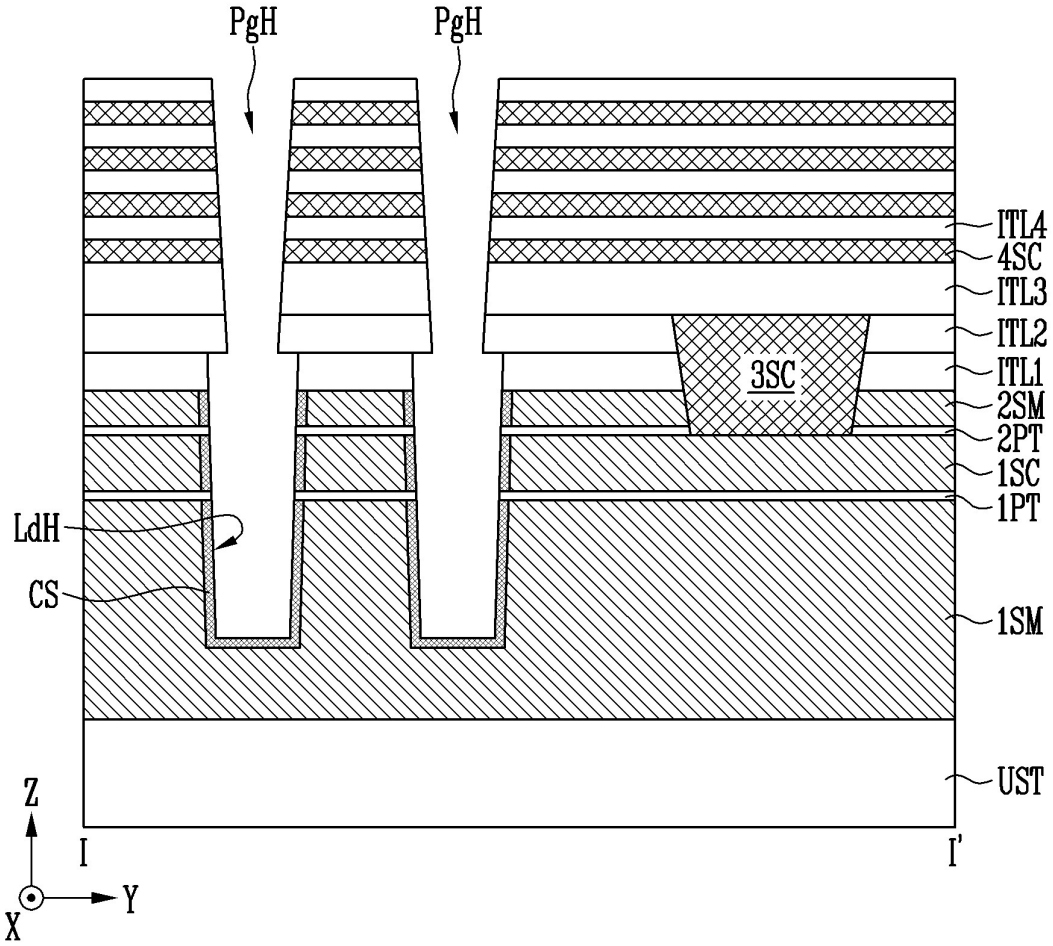

PgH
PgH
ITL4
4SC
ITL3
ITL2
3SC
ITL1
2SM
2PT
1SC
1PT
LdH
CS
1SM
UST
Z
I
I'
Y
X

FIG. 6G

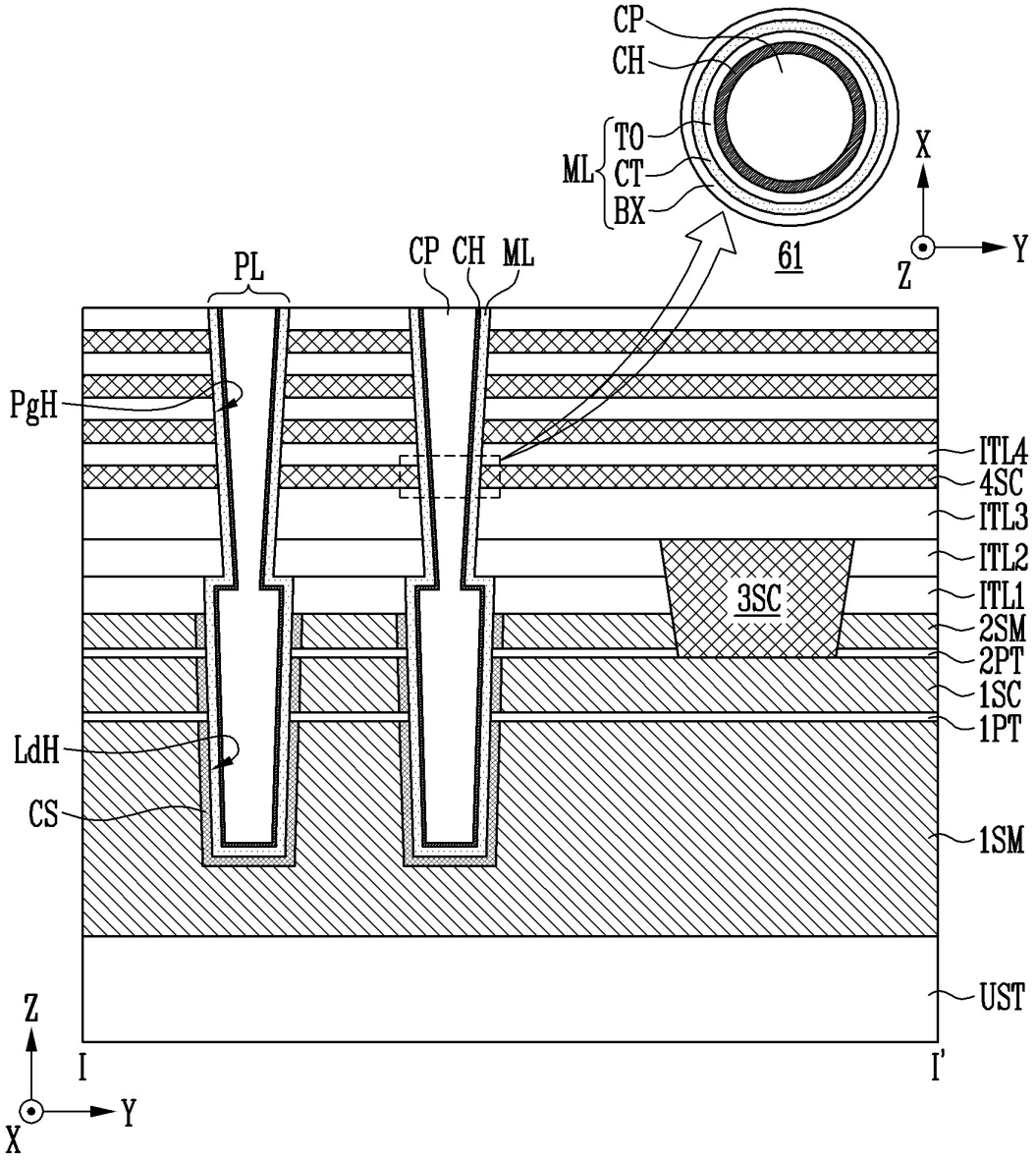

CP
CH
ML
TO
CT
BX
61
X
Y
Z
PL
CP CH ML
PgH
LdH
CS
ITL4
4SC
ITL3
ITL2
ITL1
3SC
2SM
2PT
1SC
1PT
1SM
UST
Z
I
I'
Y
X

FIG. 6H

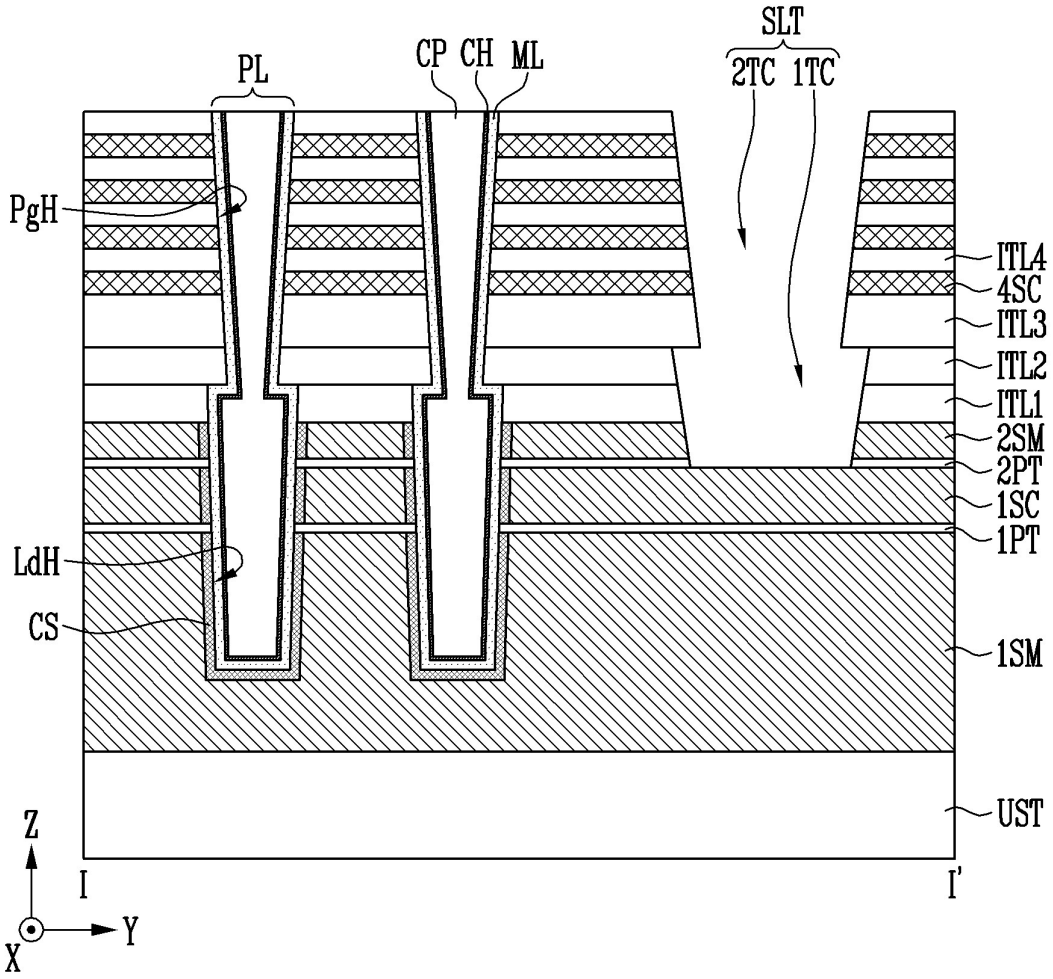

SLT
2TC 1TC
PL
CP CH ML
PgH
ITL4
4SC
ITL3
ITL2
ITL1
2SM
2PT
1SC
1PT
LdH
CS
1SM
UST
Z
I
I'
Y
X

FIG. 6I

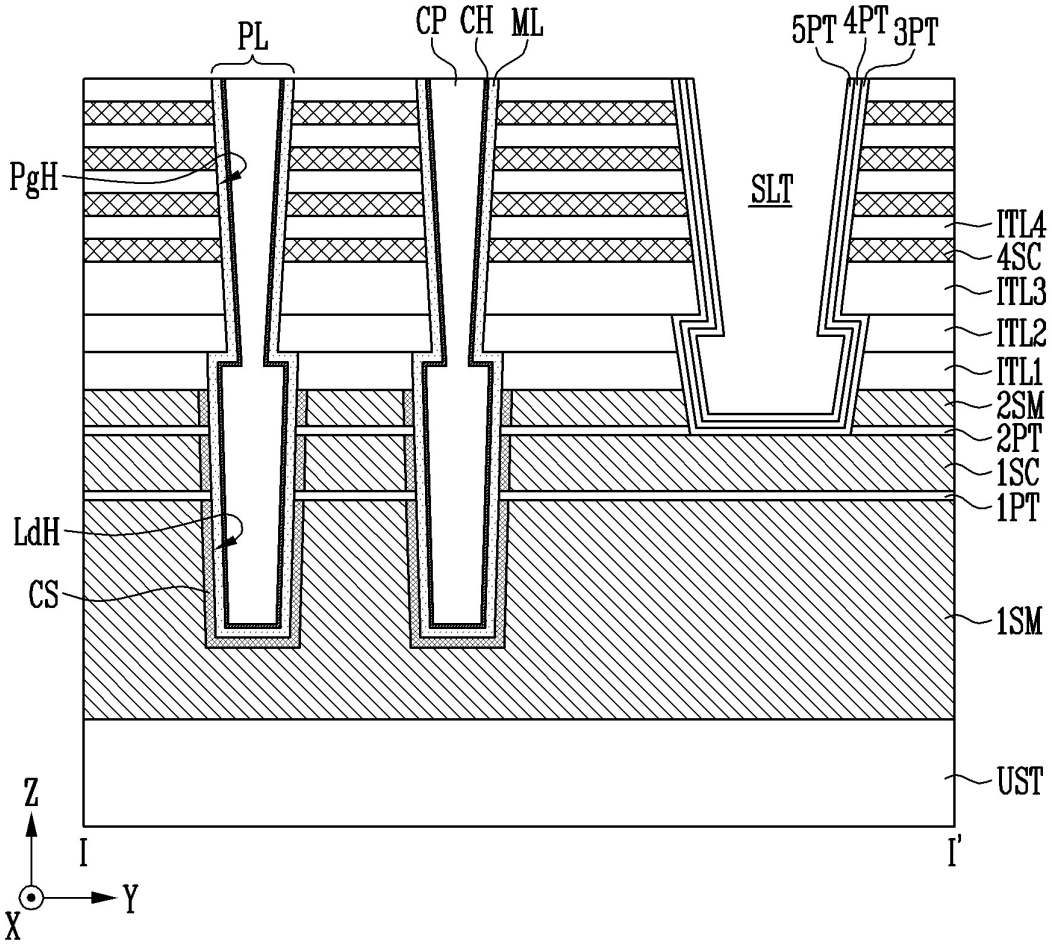

PL
CP
CH
ML
5PT
4PT
3PT
PgH
SLT
ITL4
4SC
ITL3
ITL2
ITL1
2SM
2PT
1SC
1PT
LdH
CS
1SM
UST
Z
I
I'
Y
X

FIG. 6J

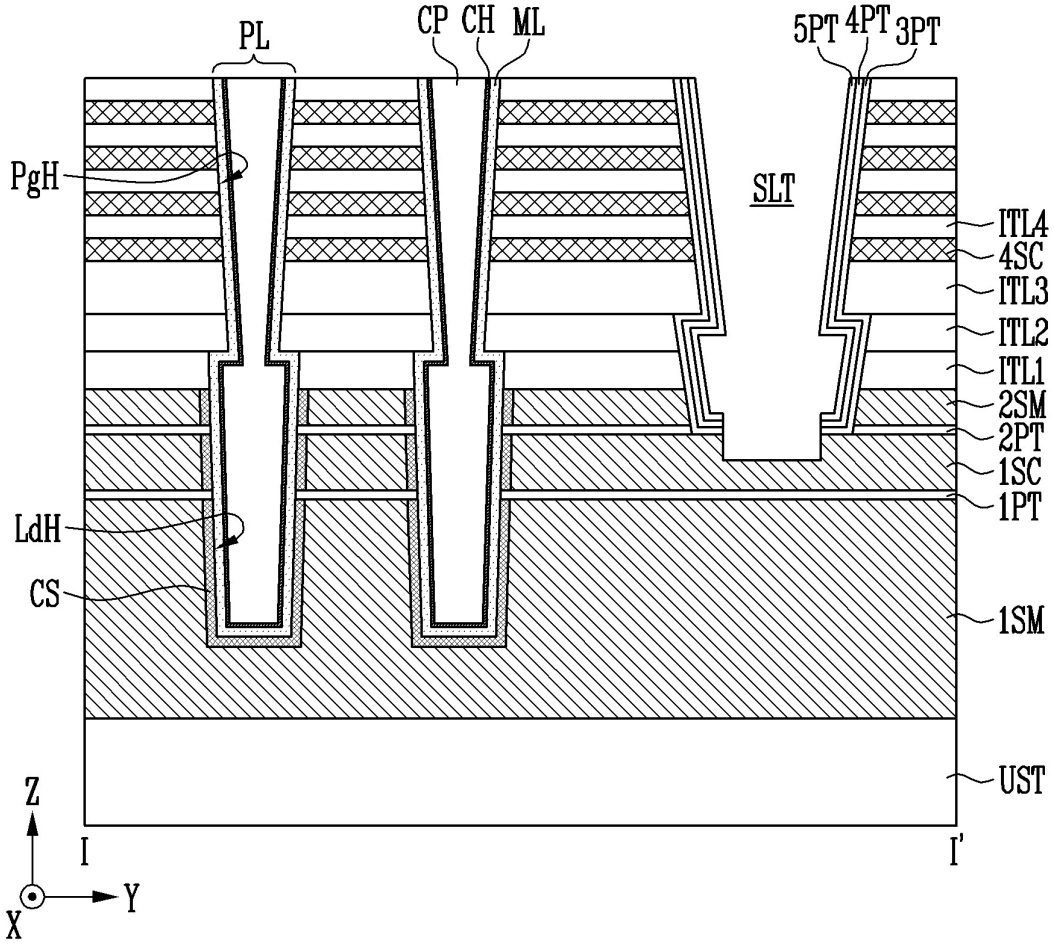

PL
CP
CH
ML
5PT
4PT
3PT
PgH
SLT
ITL4
4SC
ITL3
ITL2
ITL1
2SM
2PT
1SC
1PT
LdH
CS
1SM
UST
Z
I
I'
Y
X

FIG. 6K

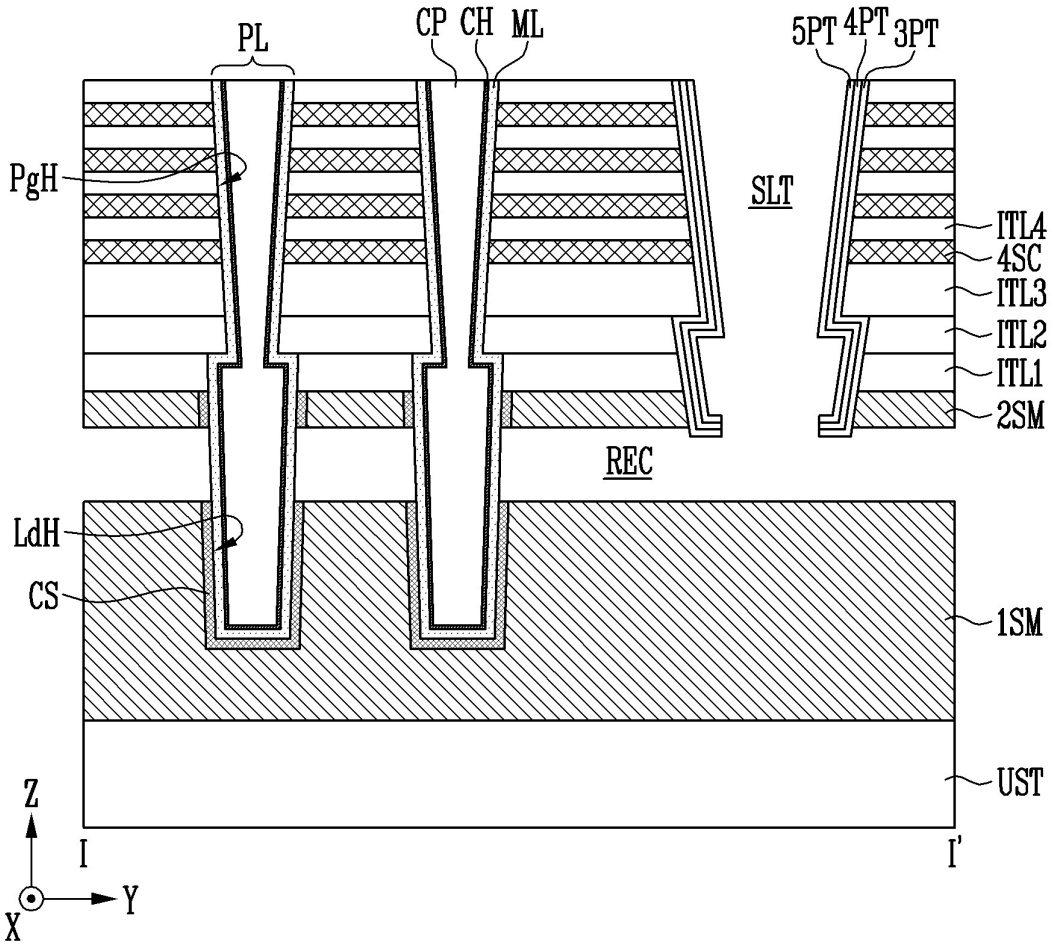

PL
CP
CH
ML
5PT
4PT
3PT
PgH
SLT
ITL4
4SC
ITL3
ITL2
ITL1
2SM
REC
LdH
CS
1SM
UST
Z
I
I'
Y
X

FIG. 6L

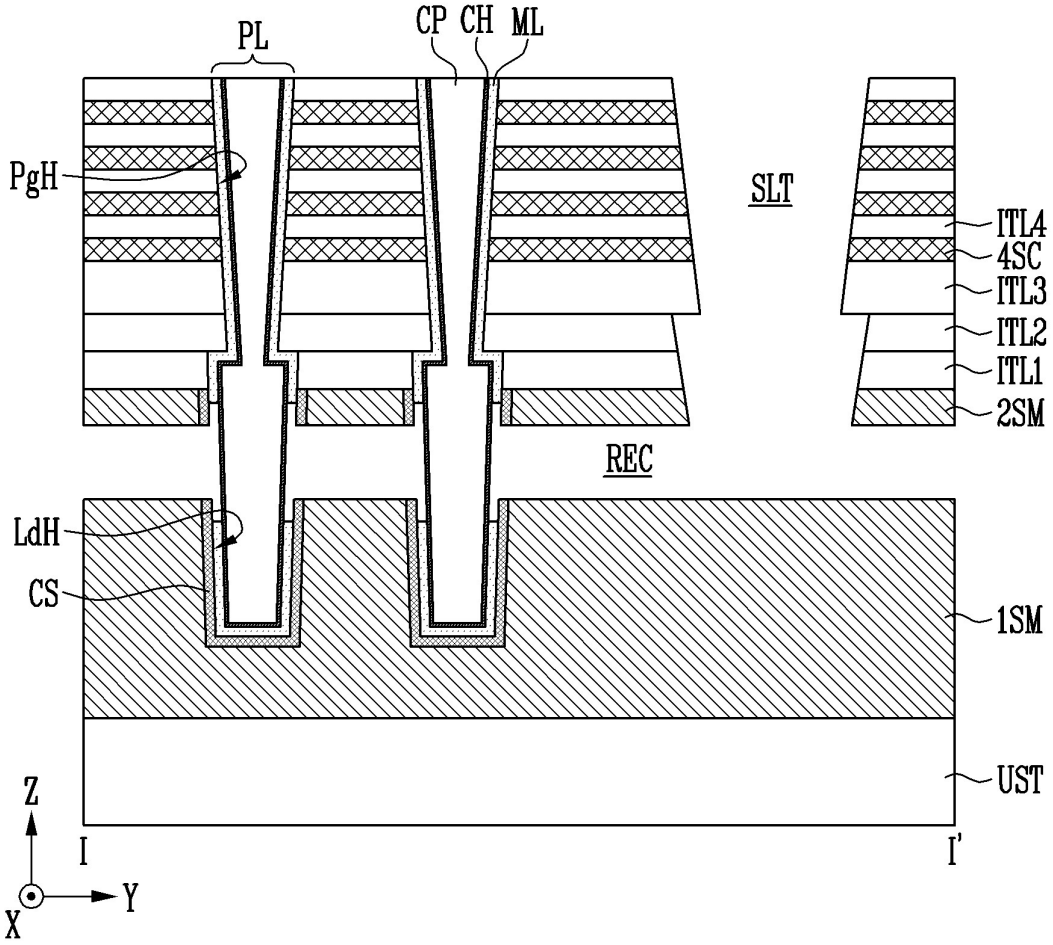

PL
CP
CH
ML
PgH
SLT
ITL4
4SC
ITL3
ITL2
ITL1
2SM
REC
LdH
CS
1SM
UST
Z
I
I'
X
Y

FIG. 6M

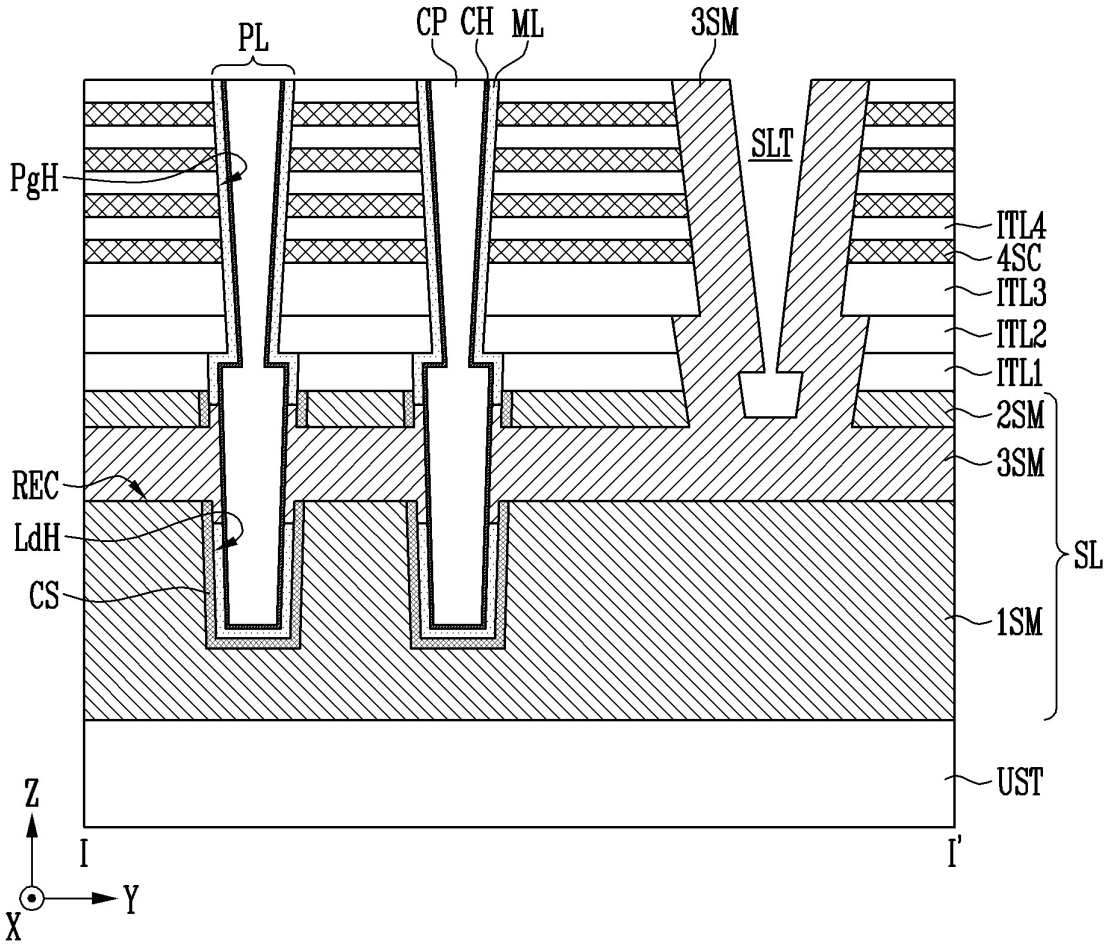

PL
CP
CH
ML
3SM
SLT
PgH
ITL4
4SC
ITL3
ITL2
ITL1
2SM
3SM
REC
LdH
CS
SL
1SM
UST
Z
I
I'
Y
X

FIG. 6N

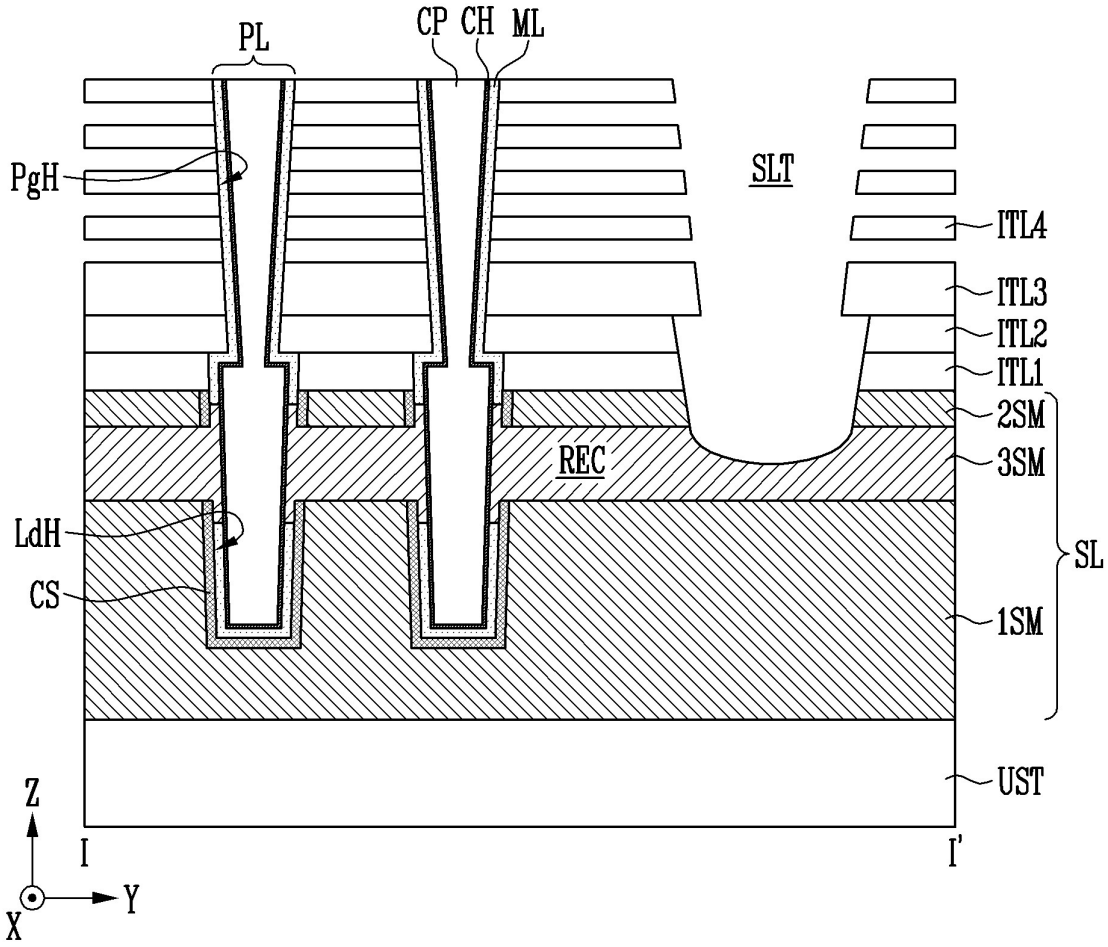

PL
CP CH ML
PgH
SLT
ITL4
ITL3
ITL2
ITL1
2SM
3SM
REC
LdH
CS
SL
1SM
UST
Z
I
I'
Y
X

FIG. 60

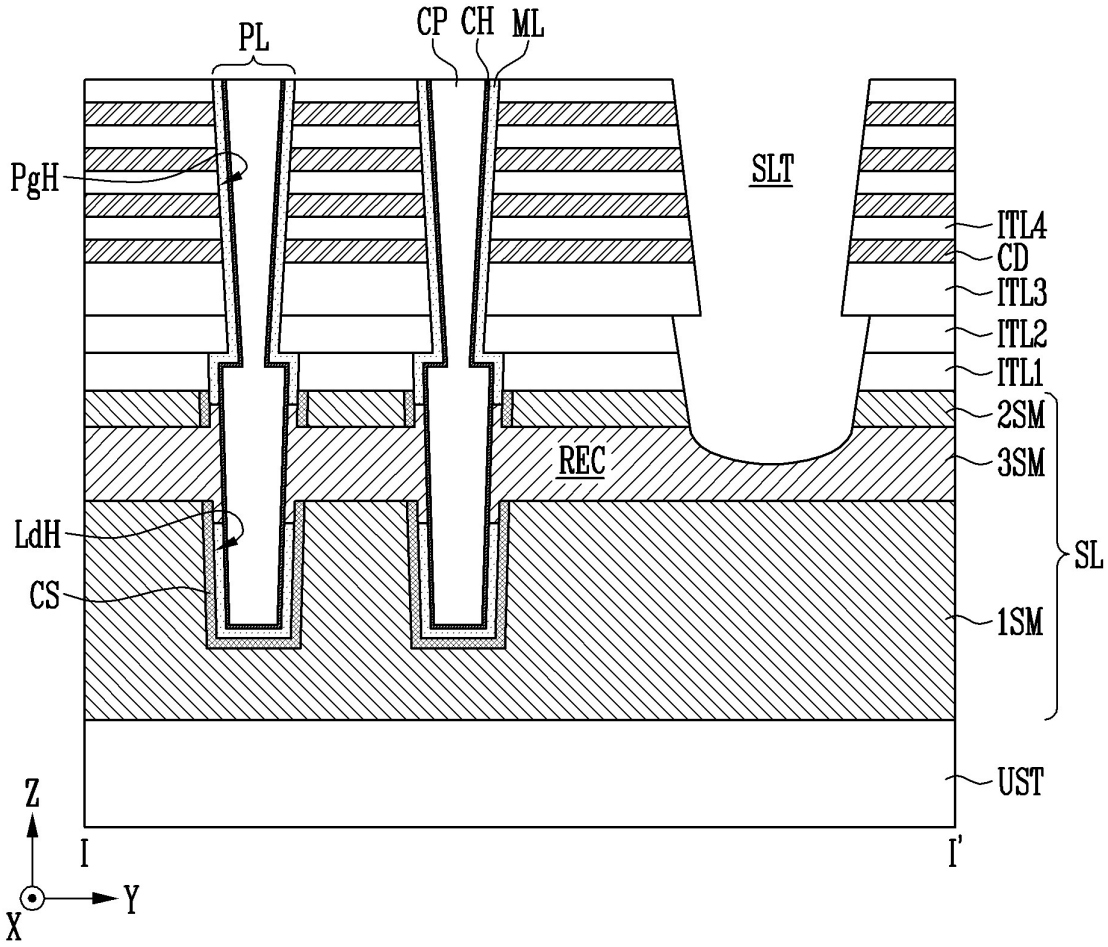

PL
CP CH ML
PgH
SLT
ITL4
CD
ITL3
ITL2
ITL1
2SM
REC
3SM
LdH
CS
SL
1SM
UST
Z
I
I'
Y
X

FIG. 6P

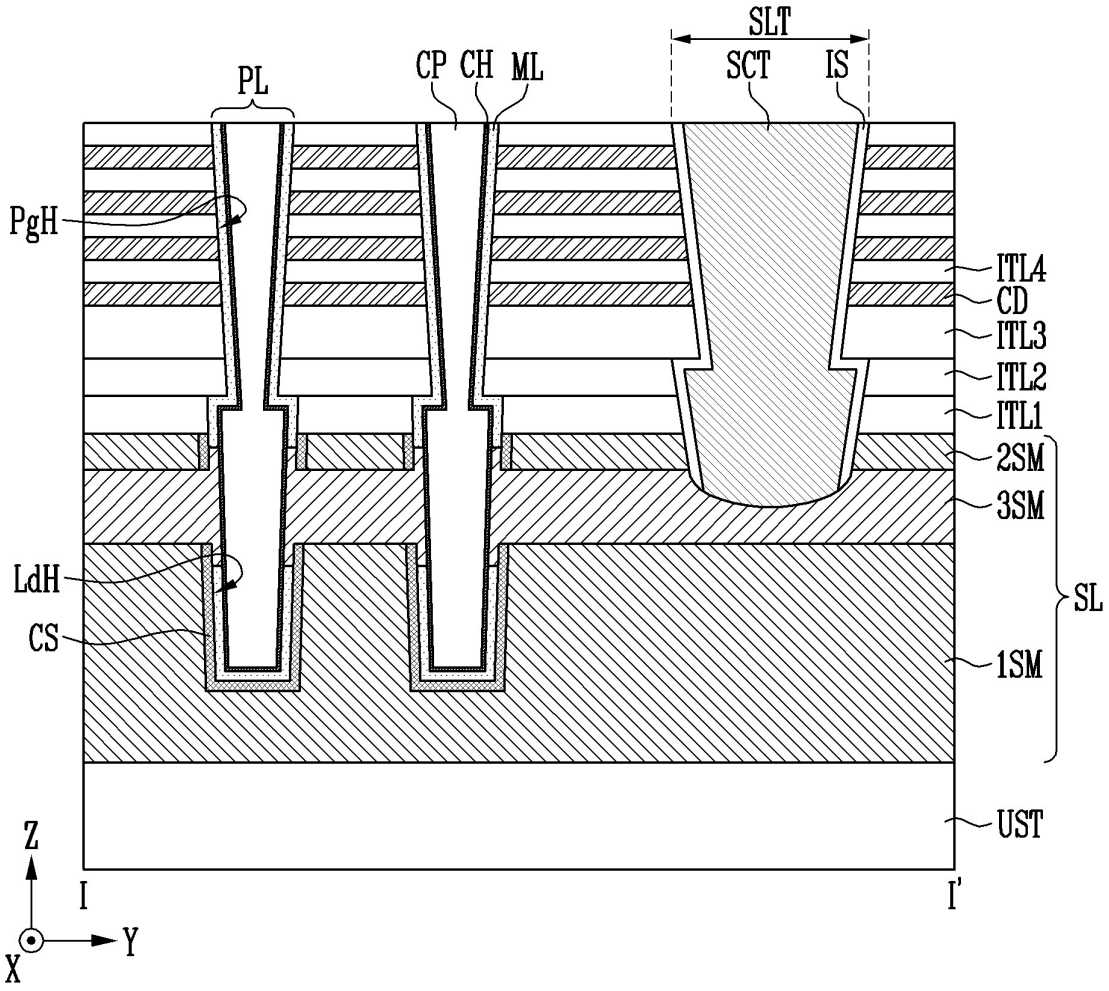

SLT
SCT
IS
PL
CP
CH
ML
PgH
ITL4
CD
ITL3
ITL2
ITL1
2SM
3SM
LdH
CS
SL
1SM
UST
Z
I
I'
Y
X

FIG. 7

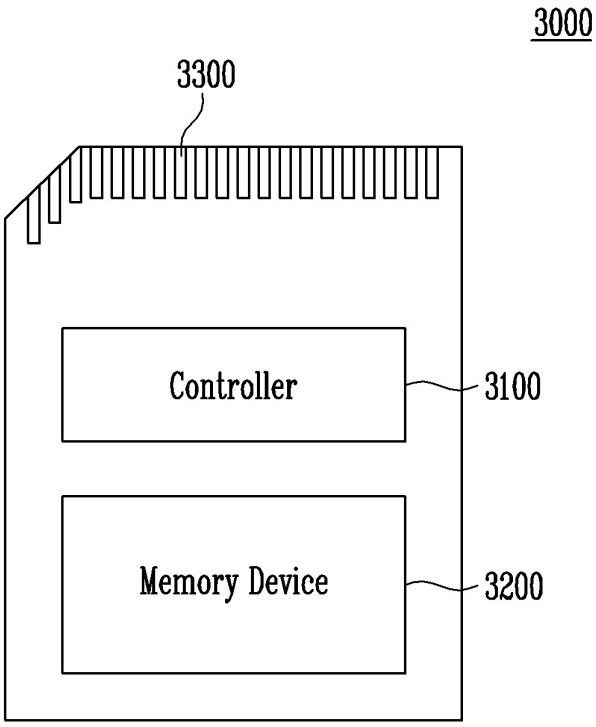
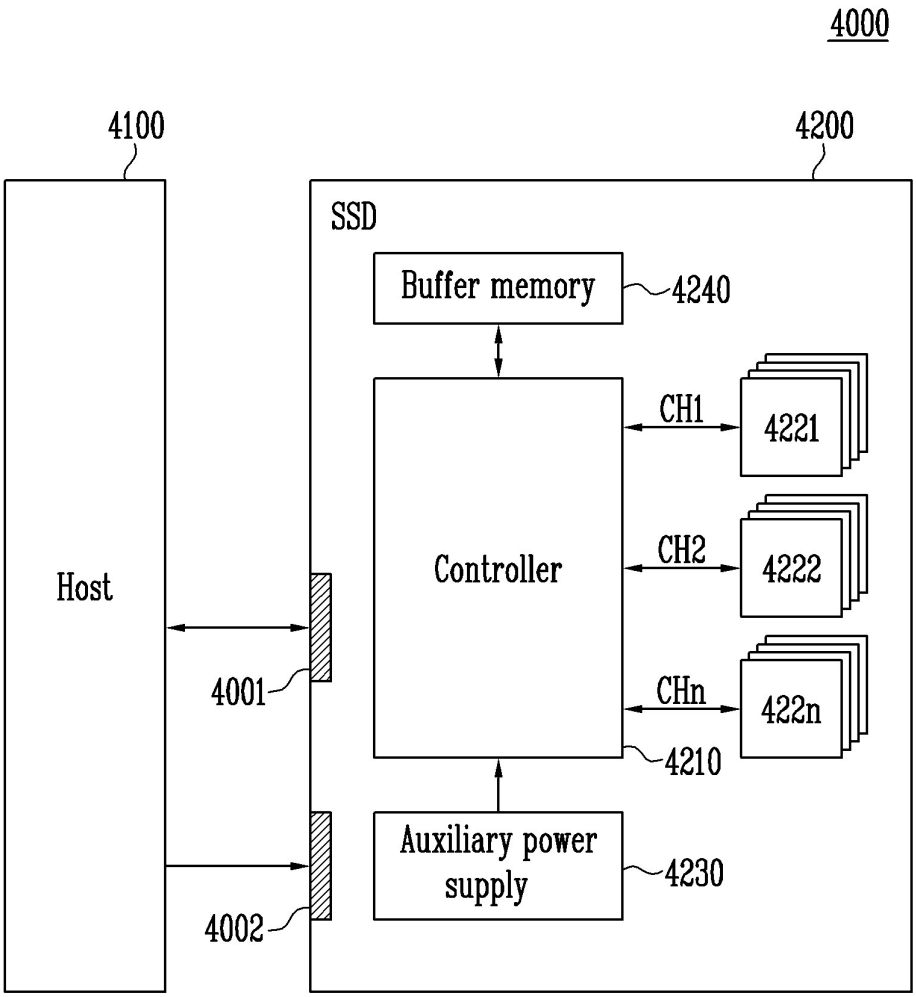


FIG. 8


4000
4100
4200
SSD
Buffer memory
4240
Controller
CH1
4221
CH2
4222
CHn
422n
4210
Host
4001
4002
Auxiliary power supply
4230