

WAFER-LEVEL CHIP MANUFACTURING METHOD

CROSS-REFERENCE TO RELATED APPLICATION

This application claim priority to Chinese Patent Application No.202410944600.7 filed
5 on Jul.7,2024,the entire content of which is incorporated herein by reference.

TECHNICAL FIELD

The present invention relates to the field of semiconductor device packaging, and more
particularly to a wafer-level chip manufacturing method.

BACKGROUND

A System-in-Package (SiP) can integrate multiple active components having different
functions, as well as passive components, micro-electro-mechanical systems (MEMS),
optical elements, and other devices into a single unit to form a system or subsystem
15 capable of providing multiple functions, thereby enabling heterogeneous IC integration.

This approach effectively addresses the limitation of System-on-Chip (SoC) technology,
which cannot easily integrate analog, radio-frequency (RF), and digital functions on the
same die.

SiP integration is relatively simple, offering shorter design and time-to-market cycles and
20 lower cost, while supporting the implementation of more complex systems.

In the existing technology, during chip packaging, chips are first bonded to one side of a
wafer without being electrically connected to the wafer.

A molding process is then performed to encapsulate and fix the chips. Subsequently, Via
are formed on the other side of the wafer, with conductive structures deposited therein to

electrically connect to the chips, allowing electrical signals from the chips to be led out through the conductive structures.

However, after molding, the wafer tends to warp significantly, making it difficult to achieve narrow linewidths during lithography, and even leading to handling issues on lithography equipment.

Accordingly, how to improve SiP integration density, achieve finer linewidths, and enhance yield remains a key technical challenge.

SUMMARY

The present invention disclosure relates to a wafer-level chip manufacturing method, including:

providing a first wafer including at least two identical first bare dies arranged in an array, each bare die having I/O metal pads on its surface;

forming a first bonding layer on the first wafer;

providing a second wafer and at least four second chips, each second chip having a device layer and an electrode layer electrically connected to the device layer;

bonding the second chips to the second wafer such that at least two of the second chips correspond in position to the first bare dies, with the electrode layer of each second chip facing away from the second wafer;

forming a first dielectric layer on the second wafer on which the second chips are bonded; etching the first dielectric layer to form Via, and depositing a conductive material therein to form first vertical conductive plugs electrically connected to the electrodes of the second chips;

forming a horizontal conductive structure on the first dielectric layer, electrically connected to the first vertical conductive plugs.

forming a second dielectric layer on the first dielectric layer and the horizontal conductive structure to form a second reconstituted wafer;

bonding the second reconstituted wafer to the first wafer such that the second dielectric layer of the second reconstituted wafer faces the first bonding layer of the first wafer, and
5 at least two of the second chips correspond respectively to the first bare dies;

removing the second wafer;

etching the first and second dielectric layers to form Via exposing the horizontal conductive structure and the I/O metal pads, and filling the Via with conductive material to form second vertical conductive plugs.

10 Through reconstitution of the second wafer and electrical interconnection between the second wafer and the first wafer, the invention achieves interconnection among devices fabricated by different semiconductor processes, thereby reducing chip area and enhancing device reliability.

15 **BRIEF DESCRIPTION OF DRAWINGS**

FIG. 1 is a flow diagram illustrating a wafer-level chip manufacturing method according to one embodiment of the present invention;

FIGS. 2–FIGS.6 are schematic cross-sectional views illustrating a wafer-level chip manufacturing method according to one embodiment of the present invention.

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DETAILED DESCRIPTION

In order to make the purposes, technical solutions and advantages of the present disclosure clearer, the present disclosure will be further explained in detail through the accompanying drawings and examples. However, it should be understood that the specific
25 embodiments described herein are only used to explain the present disclosure, and are not

used to limit the scope of the present disclosure. Further, in the following description, descriptions of well-known structures and technologies are omitted to avoid unnecessarily confusing the concepts of the present disclosure.

The preferred embodiments of the present invention are described in greater detail below.

5 Although the following description sets forth preferred embodiments of the invention, it should be understood that the invention may be implemented in various forms and should not be limited to the specific embodiments described herein.

Unless otherwise stated, directional terms such as “upper” and “lower” generally refer to the orientation of the device under normal operating conditions.

10 The terms “inner” and “outer” refer to directions relative to the device profile.

In addition, the terms “first,” “second,” and “third” are used for descriptive purposes only and should not be construed as indicating or implying relative importance, or as limiting the number of the indicated technical features. Accordingly, features defined as “first,” “second,” or “third” may explicitly or implicitly include one or more of such features. In

15 the present description, the term “plurality” means two or more, unless specifically defined otherwise. As the present invention relates to electrical devices, the terms “connection” and “interconnection” both refer to electrical interconnection. Since the drawings describe the same apparatus, identical reference numerals denote identical components throughout the figures.

20 In one embodiment, a wafer-level chip manufacturing method is provided, comprising the following steps:

Providing a first wafer, wherein the first wafer includes at least two identical first bare dies arranged in an array, each bare die having I/O metal bonding pads on its surface;

Forming a first bonding layer on the first wafer;

Providing a second wafer and at least four second chips, each second chip comprising a device layer and an electrode layer electrically connected to the device layer;

Bonding the second chips to the second wafer such that at least two of the second chips correspond in position to the first bare dies, and the electrode layers of the second chips face away from the second wafer;

Forming a first dielectric layer on the second wafer with the bonded second chips;

Etching the first dielectric layer to form Via, and depositing a conductive material therein to form first vertical conductive plugs electrically connected to the electrodes of the second chips;

Forming horizontal conductive interconnection structures on the first dielectric layer, the horizontal conductive structures being electrically connected to the first vertical conductive plugs;

Forming a second dielectric layer on the first dielectric layer and the horizontal conductive interconnection structures to form a second reconstituted wafer;

Bonding the second reconstituted wafer to the first wafer such that the second dielectric layer of the second reconstituted wafer faces the first bonding layer of the first wafer, and at least two of the second chips correspond respectively to the first bare dies;

Removing the second wafer;

Etching the first dielectric layer and the second dielectric layer to form Via exposing the horizontal conductive structure and the I/O metal bonding pads, and forming a conductive material in the Via to create second vertical conductive plugs.

In one embodiment, the material of the second dielectric layer is the same as that of the first bonding layer, and during the bonding process between the first wafer and the second wafer, the first bonding layer and the second bonding layer are joined together.

In one embodiment, a second bonding layer is further formed on the second dielectric layer.

In one embodiment, the first wafer and the second wafer are of the same size, and their edges coincide during the bonding process.

5 In one embodiment, after removal of the second wafer, the process further includes removing the bonding material between the second chips and the second wafer.

In one embodiment, the materials of the first dielectric layer and the second dielectric layer are different.

10 In one embodiment, the step of etching the first dielectric layer and the second dielectric layer to form Via comprises:

Etching the second dielectric layer to form a first sub-via that exposes an edge of the horizontal conductive structure; and

15 Further etching to form a second sub-via connected to the first sub-via, the second sub-via terminating at the surface of the I/O metal bonding pad, wherein the cross-sectional area of the second sub-via is larger than that of the exposed portion of the horizontal conductive structure.

In one embodiment, the step of etching the first dielectric layer and the second dielectric layer to form Via requires optical alignment.

20 In one embodiment, the first dielectric layer is silicon dioxide (SiO_2), and the second dielectric layer is silicon nitride (SiN_x).

In one embodiment, the second vertical conductive plugs are located in the peripheral region of the second chips.

In one embodiment, prior to etching the first and second dielectric layers to form Via, the method further comprises:

Providing a third wafer substrate and third chips, each third chip having a device layer and an electrode layer electrically connected thereto;

Bonding the third chips onto the third wafer substrate, wherein the positions of the third chips correspond to those of the first bare dies and second chips, and the electrode layers of the third chips face away from the third wafer;

Forming a first dielectric layer on the third wafer substrate on which the third chips are bonded;

Etching the first dielectric layer to form Via, and depositing a conductive material therein to form first vertical conductive plugs electrically connected to the electrodes of the third chips;

Forming horizontal conductive interconnection structures on the first dielectric layer that are electrically connected to the first vertical conductive plugs;

Forming a second dielectric layer on the first dielectric layer and the horizontal conductive interconnection structures to form a third wafer;

Forming a third bonding layer on the second wafer;

Bonding the third wafer to the second wafer such that the second dielectric layer of the third wafer faces the third bonding layer of the first wafer;

Removing the third wafer.

Referring to the drawings, the embodiments of the invention are described in detail below.

FIG. 1 shows a flow chart illustrating a wafer-level chip fabrication method according to one embodiment of the present invention. As shown in FIG. 1, the wafer-level chip fabrication method comprises the following steps:

S10: Providing a first wafer, wherein the first wafer comprises at least two first bare dies arranged in an array, and each bare die includes I/O metal bonding pads on its surface.

Specifically, as shown in FIG. 2, the first wafer 100 includes a semiconductor substrate 100, which may be made of silicon (Si), germanium (Ge), silicon-germanium (SiGe), silicon carbide (SiC), silicon-germanium-carbon (SiGeC), indium arsenide (InAs), gallium arsenide (GaAs), indium phosphide (InP), or other III-V compound semiconductors.

In this embodiment, the substrate is silicon, and an epitaxial layer 101 is formed on the silicon substrate. A plurality of first bare dies 102, consisting of semiconductor devices arranged in an array, are formed within the epitaxial layer 101 and the silicon substrate 100. For example, the first bare dies 102 may include MOS transistor logic circuits, MEMS devices, or sensors.

An insulating layer 103, made of materials such as silicon dioxide (SiO₂) or silicon nitride (Si₃N₄), is formed on the epitaxial layer 101 to cover the semiconductor devices. Metal bonding pads 104 electrically connected to the semiconductor devices are formed on the insulating layer Via 105.

S20: Forming a first bonding layer on the first wafer.

Specifically, the first bonding layer may be silicon dioxide, which becomes thermoplastic upon heating.

S30: Providing a second wafer and at least four second chips, wherein each second chip comprises a device layer and an electrode layer electrically connected thereto.

Specifically, the second wafer may be made of Si, Ge, SiGe, SiC, SiGeC, InAs, GaAs, InP, or other III-V compound semiconductors.

In this embodiment, the second wafer is a silicon wafer. The second chips may include MOS transistor logic circuits, MEMS devices, or sensors. Preferably, the second chips are fabricated by semiconductor processes different from those of the first bare dies, thereby

enabling heterogeneous wafer-level integration and overcoming the limitations of differing process technologies and packaging-induced volume increase.

S40: Bonding the second chips onto the second wafer such that at least two second chips correspond in position to the first bare dies, and the electrode layers of the second chips face away from the second wafer.

As shown in FIG. 3, a second bonding layer may be formed on the second wafer 200. The second bonding layer can be a thermally decomposable film or a UV-releasable adhesive film. The thermal-release film loses adhesion at specific temperatures (e.g., 70–80°C, 200°C, or above 400°C depending on the material), while the UV-release film loses adhesion when exposed to ultraviolet light.

The second chips 210 are bonded onto the second wafer 200 via the second bonding layer. The second wafer 200 serves as a carrier substrate for the bonding of the second chips 210 to the first bare dies 102. Therefore, the position of each second chip 210 must correspond to that of a first bare die on the first wafer.

S50: Forming a first dielectric layer 220 on the second wafer 200 having the second chips 210 bonded thereon.

As shown in FIG. 3, after bonding the second chips 210, a dielectric material is filled over the wafer to form a first dielectric layer 220. The first dielectric layer 220 provides protection and mechanical support for the second chips 210 and serves as a base for subsequent bonding and interconnection processes.

The dielectric layer 220 may include one or more of the following materials: SiO₂, Si₃N₄, epoxy resin, silicone, polyimide, benzocyclobutene (BCB), phosphosilicate glass (PSG), or fluorinated glass (FSG).

S60: Etching the first dielectric layer 220 to form vias, and depositing conductive material into the vias to form first vertical conductive plugs 230 connected to the electrode layers 201 of the second chips.

As shown in FIG. 4, the dielectric layer 220 may be etched by dry or wet etching to form Via aligned with the electrodes of the second chips.

Then, conductive materials are deposited by chemical vapor deposition (CVD), physical vapor deposition (PVD), or electroplating.

The conductive material may include one or more of the following metals: Mo, Al, Cu, W, Ta, Pt, Ru, Rh, Ir, Cr, Ti, Au, Os, Re, or Pd, or a laminated structure thereof.

S70: Forming a horizontal conductive structure 240 on the first dielectric layer 220, electrically connected to the first vertical conductive plugs 230.

As shown in FIG. 3, the horizontal conductive structure 240 may be formed by CVD, PVD, or electroplating using the same types of metal materials as described in step S60. In this embodiment, one end of the horizontal conductive structure 240 extends to the periphery of the second chip 210 for later interconnection with the first bare dies.

S80: Forming a second dielectric layer 250 on the first dielectric layer 220 and the horizontal conductive structure 240 to form a second reconstructed wafer.

As shown in FIG. 4, the second dielectric layer 250 provides interlayer insulation and mechanical support for subsequent bonding steps. The material of the second dielectric layer 250 may include one or more of SiO₂, Si₃N₄, epoxy, silicone, polyimide, BCB, PSG, or FSG. Preferably, the second dielectric layer and the first dielectric layer are made of different materials—for example, the first layer being SiO₂ and the second being Si₃N₄ or photoresist—so that selective etching of vias can be executed in multiple steps to achieve vias of different geometries.

S90: Bonding the second reconstructed wafer to the first wafer, such that the second dielectric layer of the reconstructed wafer faces the first bonding layer of the first wafer, and at least every two second chips correspond to one first bare die.

As shown in FIG. 5, since this invention provides a novel wafer-level chip fabrication method, the first and second wafers are of the same size. During bonding, the edges of the wafers are aligned, and the positions of the first and second chips are aligned optically. In the direction perpendicular to the wafer surface, the I/O metal pads of the first wafer overlap or partially overlap with the horizontal conductive structures. For example, as shown in FIG. 6, one horizontal conductive structure 2011 fully overlaps the I/O pad in projection, while another 2012 partially overlaps.

A third bonding layer is formed on the second reconstructed wafer, made of the same material as the first bonding layer. The first and third bonding layers are then brought into contact and thermally fused at high temperature to achieve wafer bonding.

S100: Removing the second wafer.

As shown in FIG. 6, since the second bonding layer is a thermally or UV-releasable film, it loses adhesion either under high temperature (e.g., 70–80°C, 200°C, or above 400°C depending on the material) or under ultraviolet exposure, allowing the second wafer to be detached.

S110: Etching the first and second dielectric layers to form Via exposing the horizontal conductive structures and I/O metal pads, and depositing conductive material into the holes to form second vertical conductive plugs.

As shown in FIG. 6, optical alignment is used to etch the dielectric layers.

A first sub-via is etched through the first dielectric layer to expose the horizontal conductive structure 2011; a second sub-via is then etched through the second dielectric layer to expose the I/O metal pad.

In another embodiment, the via diameters may differ to enable stepwise etching and prevent damage to the conductive layer.

The vias are then filled with conductive materials (Mo, Al, Cu, W, Ta, Pt, Ru, Rh, Ir, Cr, Ti, Au, Os, Re, Pd, or a laminated combination thereof) by CVD, PVD, or electroplating.

5 In another embodiment, prior to forming the vias, a third wafer substrate and third chips having electrode layers may be bonded in the same manner, repeating the aforementioned steps to achieve multi-layer wafer stacking and interconnection.

In a further embodiment, the first and second wafers are diced into multiple devices, each device comprising at least one first bare die and at least two second chips.

10 The embodiments described above are merely exemplary and should not be construed as limiting the scope of the present application.

Any equivalent structural or process variations made based on the teachings of this specification and the drawings, including the combination of features among the embodiments, or direct or indirect application in related technical fields, shall fall within

15 the protection scope of the present invention.

CLAIMS

1. A wafer-level chip manufacturing method, comprising:

providing a first wafer including at least two identical first bare dies arranged in an array,

5 each bare die having I/O metal pads on its surface;

forming a first bonding layer on the first wafer;

providing a second wafer and at least four second chips, each of the second chips having a device layer and an electrode layer electrically connected to the device layer;

10 bonding the second chips onto the second wafer such that positions of at least two of the second chips correspond to those of the first bare dies, with the electrode layer of each second chip facing away from the second wafer;

forming a first dielectric layer on the second wafer on which the second chips are bonded;

etching the first dielectric layer to form Via, and depositing a conductive material in the Via to form first vertical conductive plugs electrically interconnected with the electrodes

15 of the second chips;

forming a horizontal conductive structure on the first dielectric layer, the horizontal conductive structure being interconnected with the first vertical conductive plugs;

forming a second dielectric layer on the first dielectric layer and the horizontal conductive structure to form a second reconstituted wafer;

20 bonding the second reconstituted wafer with the first wafer such that the second dielectric layer of the second reconstituted wafer faces the first bonding layer of the first wafer, and at least two of the second chips correspond respectively to the first bare dies;

removing the second wafer;

etching the first and second dielectric layers to form Via connecting the horizontal conductive structure and the I/O metal pads, and forming a conductive material in the Via to form second vertical conductive plugs.

5 2. The wafer-level chip manufacturing method of claim 1, wherein the material of the second dielectric layer is identical to that of the first bonding layer, and during the bonding of the second reconstituted wafer and the first wafer, the first bonding layer and a second bonding layer are adhered together.

10 3. The wafer-level chip manufacturing method of claim 1, wherein further comprising forming a second bonding layer on the second dielectric layer.

4. The wafer-level chip manufacturing method of claim 2, wherein the first wafer and the second wafer have identical dimensions, and are aligned at their edges during bonding.

15 5. The wafer-level chip manufacturing method of claim 3, wherein after removal of the second wafer, the bonding material between the second chips and the second wafer is further removed.

20 6. The wafer-level chip manufacturing method of claim 4, wherein the first dielectric layer and the second dielectric layer are made of different materials.

7. The wafer-level chip manufacturing method of claim 5, wherein the step of etching the first and second dielectric layers to form Via comprises:

etching the second dielectric layer to form first sub-Via that expose the edges of the horizontal conductive structure;

further etching to form second sub-Via connected to the first sub-Via, the second sub-Via stopping at the surface of the I/O metal pads, wherein a cross-sectional area of each second sub-Via is bigger than that of the exposed portion of the horizontal conductive structure.

8. The wafer-level chip manufacturing method of claim 6, wherein the step of etching the first and second dielectric layers to form Via is performed using optical alignment.

9. The wafer-level chip manufacturing method of claim 7, wherein the second vertical conductive plugs are located in peripheral regions of the second chips.

10. The wafer-level chip manufacturing method of claim 8, wherein further comprising, before the step of etching the first and second dielectric layers to form Via:

providing a third wafer substrate and third chips, each third chip having a device layer and an electrode layer electrically connected to the device layer;

bonding the third chips onto the third wafer substrate such that positions of the third chips correspond respectively to those of the first bare dies and the second chips, with the electrode layers of the third chips facing away from the third wafer substrate;

forming a first dielectric layer on the third wafer substrate on which the third chips are bonded;

etching the first dielectric layer to form Via, and depositing conductive material therein to form first vertical conductive plugs electrically connected to the electrodes of the third chips;

forming a horizontal conductive structure on the first dielectric layer interconnected with the first vertical conductive plugs;

forming a second dielectric layer on the first dielectric layer and the horizontal conductive structure to form a third wafer;

5 forming a third bonding layer on the second reconstituted wafer;

bonding the third wafer with the second reconstituted wafer such that the second dielectric layer of the third wafer faces the third bonding layer of the first wafer;

and removing the third wafer substrate.