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# NEW BACK-END CAPACITOR WITH HIGH UNIT CAPACITANCE

## BACKGROUND OF THE INVENTION

### FIELD OF THE INVENTION

This invention deals with the formation of a capacitor having a high unit capacitance for analog circuits. Bond pads are formed at the same time the bottom capacitor plate is formed using a conducting material which will avoid bond pad peeling during subsequent processing.

### DESCRIPTION OF THE RELATED ART

Anderson et al., U.S. Pat. No. 4,495,222 shows the use of polysilicon under the bond pad to eliminate bond pad peeling during subsequent processing. In the invention of this Patent Application, however, a bottom capacitor plate is formed at the same time the bond pads are formed. This integrated process step provides a bond pad which will

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eliminate bond pad peeling during subsequent process steps and a capacitor with high unit capacitance for use in analog circuits. The top capacitor plate is formed at the same time the top electrode pattern is formed.

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## SUMMARY OF THE INVENTION

Capacitors with two metal plates or one metal and one polysilicon plate integrated into an integrated circuit element are often used in analog circuit applications because of their high degree of linearity. It is difficult to obtain a sufficiently large capacitance per unit area in these capacitors to enable them to be used without stacking.

Input/output connections for an integrated circuit elements often use a bond pad formed on a layer of dielectric material such as silicon dioxide or borophosphosilicate glass. Special care must be taken to prevent peeling of the bond pad from the dielectric material.

It is an objective of this invention to provide a method of forming a capacitor with high capacitance per unit area and simultaneously forming a bond pad interface which will prevent bond pad peeling.

It is a further objective of this invention to provide a capacitor with a high capacitance per unit area for use in analog circuits and a bond pad interface which will prevent bond pad peeling.

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These objectives are achieved by means of a bottom plate capacitor trench and a bond pad trench formed in a layer of interlevel dielectric. The interlevel dielectric is formed over a semiconductor substrate having devices formed therein. The bottom plate capacitor trench and the bond pad trench are filled with a conductor material such as doped polysilicon thereby forming a bottom capacitor plate and a bond pad. A capacitor dielectric is formed over the bottom capacitor plate and a metal top capacitor plate is formed over the capacitor dielectric. The polysilicon interface between the bond pad and the interlevel dielectric prevents bond pad peeling and the capacitor structure provides good capacitor linearity and a capacitance per unit area in excess of 0.5 femtofarads per square nanometer.

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## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a cross section view of a semiconductor substrate with the capacitor structure, bond pads, bond pad contacts, device contacts, and top metal pattern formed taken along line 1-1′ of Fig. 6.

Fig. 2 shows a cross section view of the semiconductor substrate with devices formed therein and interlevel dielectric formed thereon taken along line 1-1′ of Fig. 6.

Fig. 3 shows a cross section view of the semiconductor substrate with the bottom capacitor trench and bond pad trenches formed in the interlevel dielectric and filled with conductor material taken along line 1-1′ of Fig. 6.

Fig. 4 shows a cross section view of the semiconductor substrate with the capacitor dielectric formed over the bottom capacitor plate, the bond pad, and the interlevel dielectric taken along line 1-1′ of Fig. 6.

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Fig. 5 shows a cross section view of the semiconductor substrate with the capacitor dielectric formed over the bottom capacitor plate, the bond pad, and the interlevel dielectric, the bond pad contact holes, the bottom capacitor contact hole, and the device contact holes taken along line 1-1′ of Fig. 6.

Fig. 6 shows a top view of the capacitor structure showing device contacts and bond pad contacts.

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## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Refer now to Figs. 1-6 there is shown an embodiment of a method of forming the capacitor and bond pad structure of this invention. Fig. 2 shows a semiconductor substrate 10 with a field effect transistor formed therein. The field effect transistor comprises source/drain regions 13 and 14, a gate dielectric layer 12, a gate electrode 15, and field oxide isolation regions 11. An interlevel dielectric layer 26 is formed over the silicon substrate. The interlevel dielectric is a material such as borophosphosilicate glass or boron doped tetraethyl orthosilicate material.

As shown in Fig. 3 trenches are then formed in the interlevel dielectric for the bottom capacitor plate, the bottom capacitor contact, and the bond pads. Fig. 3 shows only one of the bond pads. The mask used for this step is the only additional mask required over the masks required to form the integrated circuit element without the capacitor. These trenches are then filled with a first conductor material to form the bottom capacitor plate 20, the bottom capacitor contact 35, and the bond pad 23. As shown in Fig. 3, the capacitor contact 35 is electrically connected to the bottom capacitor plate 23. The first conductor material is preferably a material such as doped polysilicon

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so that doped polysilicon is formed in the bond pad area as the bottom capacitor plate is formed. Polysilicon at the interface between the bond pad and the interlevel dielectric is effective in preventing bond pad peeling during subsequent processing. This is achieved without the need of extra process steps. A metal such as tungsten can also be used for the first conductor material.

Next, as shown in Fig. 4, a layer of capacitor dielectric 22 is formed over the interlevel dielectric 26, the bottom capacitor plate 20, and the bond pads 23. The capacitor dielectric is a material such as ONO, oxide nitride oxide layered structure or sandwich structure, or TEOS, tetraethyl orthosilicate, with a thickness of between about 300 and 700 Angstroms. This capacitor dielectric thickness provides a capacitance per unit area in excess of 0.5 femtofarads per square nanometer.

Next, as shown in Fig. 5, contact holes in the capacitor dielectric 22 are formed for the bond pads 24 and the bottom capacitor plate 25. Only one bond pad and one bond pad contact hole is shown, although it will be obvious to those skilled in the art that this method is equally applicable to a number of bond pad and bond pad contact holes. Contact holes are also formed in both the capacitor dielectric 22 and the interlevel dielectric 26 for device

contacts 16, 17, and 18. These contact holes are then filled with a second conducting material such as a composite of titanium/titanium nitride and tungsten.

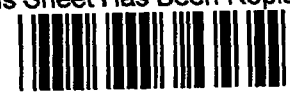
As shown in Fig. 1, a first metal electrode pattern is formed over capacitor dielectric 22, the filled bond pad contact holes 24, the bottom capacitor contact hole 25, and the filled device contact holes 16, 17, and 18. The first metal electrode pattern forms the top capacitor plate 21, the electrode 36 to one of the filled bond pad contact holes 24, the electrode 27 to the filled bottom capacitor contact hole 25, and the electrodes 31, 32, and 33 to the filled device contact holes 16, 17, and 18. The first metal electrode pattern is formed of a material such as a composite of aluminum/silicon/copper. Fig. 1 is a cross section view of the capacitor and bond pad structure taken along line 1-1' of Fig. 6.

The top view of the first metal electrode pattern is shown in Fig. 6. Fig. 6 shows the top capacitor plate 21, the electrode 36 to one of the filled bond pad contact holes 24, the electrode 27 to the filled bottom capacitor contact hole 25, the electrode 34 to the top capacitor plate 21, and the electrodes 31, 32, and 33 to the filled device contact holes 16, 17, and 18.

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In this embodiment the bottom capacitor plate and the bond pads are formed at the same time using only one extra mask beyond those masks required for the device without the capacitor. The conducting material used to form the bottom capacitor plate and the bond pads is chosen to prevent bond pad peeling when external electrodes are bonded to the bond pads.

Refer now to Figs. 1 and 6, there is shown an embodiment of the capacitor and bond pad structure of this invention. The top view of the structure is shown in Fig. 6. Fig. 6 shows the top capacitor plate 21, the electrode 36 to one of the filled bond pad contact holes 24, the electrode 27 to the filled bottom capacitor contact hole 25, the electrode 34 to the top capacitor plate 21, and the electrodes 31, 32, and 33 to the filled device contact holes 16, 17, and 18.

A cross section view of the capacitor and bond pad structure, taken along line 1-1' of Fig. 6, is shown in Fig. 1. Fig. 1 shows a semiconductor substrate 10 with a field effect transistor formed therein. The field effect transistor comprises source/drain regions 13 and 14, a gate dielectric layer 12, a gate electrode 15, and field oxide isolation regions 11. An interlevel dielectric layer 26 is formed over the silicon substrate. The interlevel

dielectric is a material such as borophosphosilicate glass or boron doped tetraethyl orthosilicate material.

Trenches are formed in the interlevel dielectric for the bottom capacitor plate, the bottom capacitor contact, and the bond pads. These trenches are then filled with a first conductor material to form the bottom capacitor plate 20, the bottom capacitor contact 35, and the bond pad 23. The capacitor contact 35 is electrically connected to the bottom capacitor plate 23. The first conductor material is preferably a material such as doped polysilicon so that doped polysilicon is formed in the bond pad area as the bottom capacitor plate is formed. Polysilicon at the interface between the bond pad and the interlevel dielectric is effective in preventing bond pad peeling during subsequent processing. This is achieved without the need of extra process steps. A metal such as tungsten can also be used for the first conductor material.

A layer of capacitor dielectric 22 is formed over the interlevel dielectric 26, the bottom capacitor plate 20, and the bond pads 23. The capacitor dielectric is a material such as ONO, oxide oxynitride, or TEOS, tetraethyl orthosilicate, with a thickness of between about 300 and 700 Angstroms. This capacitor dielectric thickness provides a capacitance per unit area in excess of 0.5 femtofarads per

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square nanometer. Contact holes are formed in the capacitor dielectric 22 for the bond pads 24 and the bottom capacitor plate 25. Only one bond pad and one bond pad contact hole is shown. Contact holes are also formed in both the capacitor dielectric 22 and the interlevel dielectric 26 for device contacts 16, 17, and 18. These contact holes are filled with a second conducting material, which in this example is also doped polysilicon.

A first metal electrode pattern is formed over capacitor dielectric 22, the filled bond pad contact holes 24, the bottom capacitor contact hole 25, and the filled device contact holes 16, 17, and 18. The metal electrode forms the top capacitor plate 21, the electrode 36 to one of the filled bond pad contact holes 24, the electrode 27 to the filled bottom capacitor contact hole 25, and the electrodes 31, 32, and 33 to the filled device contact holes 16, 17, and 18.

This capacitor and bond pad structure provides bond pads which will not peel during subsequent processing and a capacitor with a capacitance in excess of 0.5 femtofarads per square nanometer.

While the invention has been particularly shown and described with reference to the preferred

embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

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1. A method of forming a capacitor, comprising the steps of:

providing a semiconductor substrate having devices formed therein and a layer of interlevel dielectric formed thereon;

planarizing said layer of interlevel dielectric;

forming a bottom capacitor plate trench region, a bottom capacitor contact trench region, and a number of bond pad trench regions in said layer of interlevel dielectric;

filling said bottom capacitor plate trench region with a first conductor material thereby forming a bottom capacitor plate;

filling said bottom capacitor contact trench region with a first conductor material thereby forming a bottom capacitor contact;

filling said bond pad trench regions with said first conductor material thereby forming a number of bond pads;

forming a layer of capacitor dielectric over said bottom capacitor plate, said bottom capacitor contact, said bond pads, and said layer of interlevel dielectric;

forming a bottom capacitor contact hole and a number of bond pad contact holes in said capacitor dielectric, wherein said bottom capacitor contact hole is directly over said bottom capacitor contact and each said bond pad contact hole is over one of said bond pads;

forming a number of device contact holes in said capacitor dielectric and said interlevel dielectric;

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filling said bond pad contact holes, said bottom capacitor contact hole, and said device contact holes with a second conductor material;

forming a layer of third conductor material over said capacitor dielectric, said bond pad contact holes, and said device contact holes; and

patterning said layer of third conductor material to form a top capacitor plate and a top electrode pattern.

2. The method of claim 1 wherein said first conductor material is doped polysilicon.

3. The method of claim 1 wherein said first conductor material is tungsten.

4. The method of claim 1 wherein said interlevel dielectric is borophosphosilicate glass.

5. The method of claim 1 wherein said interlevel dielectric is boron doped tetraethyl orthosilicate.

6. The method of claim 1 wherein said capacitor dielectric is tetraethyl orthosilicate.

7. The method of claim 1 wherein said capacitor dielectric is oxide nitride oxide layered structure.

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8. The method of claim 1 wherein said capacitor dielectric has a thickness of between about 300 and 700 Angstroms.

9. The method of claim 1 wherein said top capacitor plate is formed directly above said bottom capacitor plate.

10. The method of claim 1 wherein said second conductor material is titanium/titanium nitride and tungsten.

11. The method of claim 1 wherein said third conductor material is aluminum/silicon/copper.

12. A capacitor structure, comprising:

a semiconductor substrate having devices formed therein and a planarized layer of interlevel dielectric formed thereon;

a bottom capacitor plate trench region, a bottom capacitor contact trench region, and a number of bond pad trench regions formed in said layer of interlevel dielectric;

a bottom capacitor plate formed by filling said bottom capacitor trench region with a first conductor material;

a bottom capacitor contact formed by filling said bottom capacitor contact trench with said first conductor material;

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a number of bond pads formed by filing said bond pad trench regions with said first conductor material;

a layer of capacitor dielectric formed over said bottom capacitor plate, said bottom capacitor contact, said bond pads, and said layer of interlevel dielectric;

a bottom capacitor contact hole and a number of bond pad contact holes formed in said capacitor dielectric;

a number of device contact holes formed in said capacitor dielectric and said interlevel dielectric;

a second conductor material filling said bond pad contact holes, said bottom capacitor contact hole, and said device contact holes;

a layer of third conductor material formed over said capacitor dielectric, said bottom capacitor contact hole, said bond pad contact holes, and said device contact holes; and

a top capacitor plate and a top electrode pattern formed in said layer of third conductor material.

13. The capacitor structure of claim 11 wherein said first conductor material is doped polysilicon.

14. The capacitor structure of claim 11 wherein said first conductor material is tungsten.

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15. The capacitor structure of claim 11 wherein said interlevel dielectric is borophosphosilicate glass.

16. The capacitor structure of claim 11 wherein said interlevel dielectric is boron doped tetraethyl orthosilicate.

17. The capacitor structure of claim 11 wherein said capacitor dielectric is tetraethyl orthosilicate.

18. The capacitor structure of claim 11 wherein said capacitor dielectric is oxide nitride oxide layered structure.

19. The capacitor structure of claim 11 wherein said capacitor dielectric has a thickness of between about 300 and 700 Angstroms.

20. The capacitor structure of claim 11 wherein said top capacitor plate is formed directly above said bottom capacitor plate.

21. The capacitor structure of claim 11 wherein said second conductor material is titanium/titanium nitride and tungsten.

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22. The capacitor structure of claim 11 wherein said third conductor material is aluminum/silicon/copper.

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