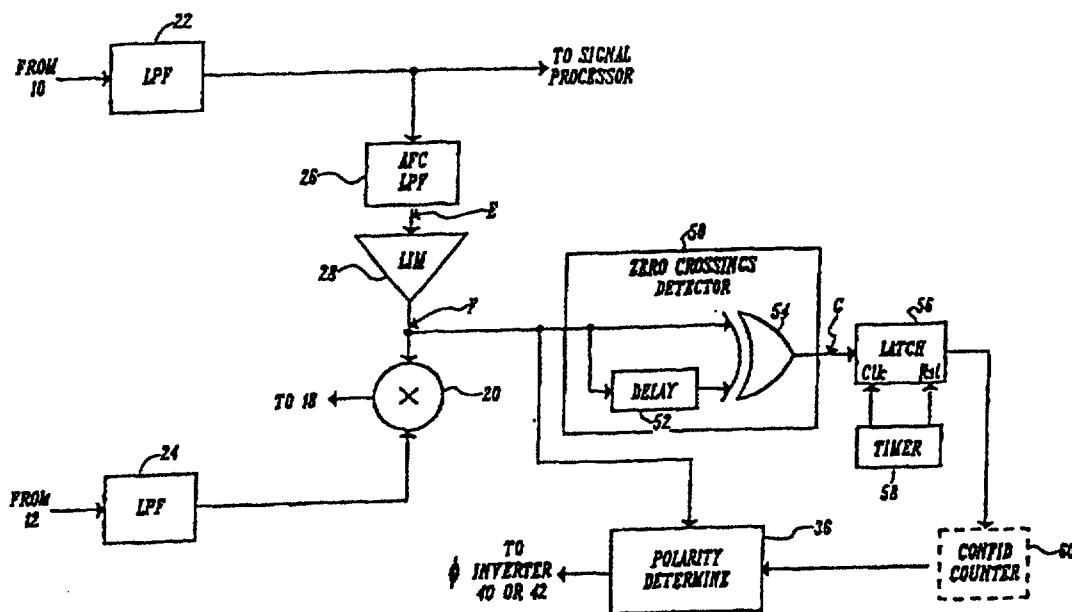


## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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| (51) International Patent Classification <sup>6</sup> :<br><b>H03D 1/00, H04L 27/06</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | <b>A1</b> | (11) International Publication Number: <b>WO 98/06173</b><br>(43) International Publication Date: <b>12 February 1998 (12.02.98)</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
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(54) Title: FREQUENCY LOCK INDICATOR FOR FPLL DEMODULATED SIGNAL HAVING A PILOT



## (57) Abstract

A biphase stable FPLL includes a polarity determination circuit (36) that ascertains the lockup phase of the FPLL based upon the polarity of the pilot in the digital signal. A frequency lock indicator circuit (50-60) determines from the recovered pilot when frequency lock has occurred and the polarity determination circuit is responsive thereto for inverting the phase of the incoming signal (or alternatively, of the outgoing signal) as determined in order to supply an output signal of predetermined polarity. The frequency lock indicator consists of a zero crossings detector (50) and a latch (56) that is sampled for a time period. The zero crossings detector (50) is a delay (52) and an exclusive OR gate (54). An optional confidence counter (60) may be used with the latch (56) to determine when frequency lock has occurred to provide the lock indicator signal.