

SPECIFICATION

Digital-to-analog converter

- 5 The present invention relates to a digital-to-analog converter (hereinafter referred to also as D-A converter in abridgement) for converting a digital signal into a corresponding analog signal.
- 10 In order to have a better understanding of the invention, description will be first made of a hitherto known D-A converter by referring to Fig. 1 which is a block diagram showing a typical example of the prior art D-A converter of pulse width modulation (PWM) type. For simplification of the description, it is assumed that each digital data to be converted into a corresponding analog quantity consists of four bits and thus the counter used for the conversion is also of four-bit capacity. In Fig. 1, reference numeral 1 denotes a clock pulse generator circuit for producing clock pulses which are counted by a counter 2 having a carry output C. All the bits of digital data D_1 , D_2 , D_3 and D_4 fed to digital input terminals 4a, 4b, 4c and 4d, respectively, are compared with the bits of the outputs Q_4 , Q_3 , Q_2 and Q_1 of the counter 2 through a comparator circuit 3. When coincidence is found, the comparator circuit 3 will produce a coincidence signal. An RS flip-flop 5 has a set input terminal S connected to the carry output terminal C of the counter 2 and a reset input terminal R connected to the output terminal of the comparator circuit 3 so as to be reset by the coincidence signal output from the comparator 3. The Q-output (non-inverted output) from the RS flip-flop 5 is connected to the input of an integrator circuit 6 to be converted into a corresponding analog signal which in turn is applied to the input of a voltage conversion circuit 7 adapted to produce a corresponding voltage signal at an analog voltage output terminal 8.
- 45 Next, operation of the D-A converter of the arrangement described above will be discussed with the aid of signal waveforms illustrated in the diagram of Fig. 2. The clock pulse generator circuit 1 produces clock pulses such as shown at (a) in Fig. 2, while the counter 2 counts 16 pulses labelled "0" to "15" during a single counting cycle or period. When the contents of the counter 2 becomes "0", the carry-out signal, such as shown at (b) in Fig. 2, is produced and supplied to the set input terminal S of the RS flip-flop 5 as a set signal. Under these conditions, when a digital data input such as "0101" (which is equal to "5" according to the decimal notation), for example, which is to be converted into an analog quantity is applied to the digital input terminals 4d, 4c, 4b and 4a, then the input data is compared with the contents of the counter 2 by the comparator circuit 3, as a result of which the coinci-

- dence signal, such as shown at (c) in Fig. 2, is produced at the time when the contents of the counter 2 becomes equal to "5". The coincidence signal is then supplied to the reset input R of the RS flip-flop 5 as a reset signal. Accordingly, the RS flip-flop 5 is set when the contents of the counter 2 is equal to zero and reset when the contents of the counter 2 is equal to "5". Consequently, the Q-output signal from the RS flip-flop 5 will be as shown at (d) in Fig. 2 during a single counting cycle or period of the counter 2. Generation of such a Q-output signal is subsequently repeated for every succeeding counting cycle or period of the counter 2. The Q-output signal is converted into a DC signal by the integrator circuit 6 and finally converted into a corresponding voltage value by the succeeding voltage converter stage 7.
- 85 If the number of clock pulses counted by the counter 2 during one period (a single counting cycle) is represented by N, the input data value applied to the input terminals 4d to 4a is represented by n and a reference voltage of the voltage converter circuit 7 is represented by V_0 , then the voltage V produced at the analog signal output terminal 8 is given by the following expression:

$$95 \quad V = n/N \cdot V_0$$

This means that the analog signal voltage as obtained is proportional to the input digital data n.

- 100 In the D-A converter as described above, examination will next be made on the operation of the converter at the time when the input digital data value n undergoes variation. Referring to Fig. 3, it is assumed that a change occurs in the digital data value n at a given time point T in the course of elapse of time t. The analog output voltage will then change during a finite time Δt , which improves limits on the system for reasons described below:
- So far as $t \leq T$, $n = n_1$, and when $T < t$, $n = n_2$, wherein $n_1 < n_2$. On the above assumption, the Q-output of the RS flip-flop 5 will of course change the waveform thereof at the boundary time T as is shown at (a) in Fig. 3. However, it will be noted that the output analog voltage will not instantly change in a step-like manner because of the time constant of the integrator circuit 6, but a transient delay time Δt will intervene between the time T and the new steady level of the analog output voltage, as shown at (b) in Fig. 3. Such a delay time Δt of course depends on the time constant of the integrator circuit 6 which time constant can not however be selected at an arbitrary small value in consideration of the fact that the function of the integrator circuit 6 is to integrate the waveform of the Q-output of the RS flip-flop 5 adequately so that the integrator output is free of ripple

component.

As will be appreciated from the above discussion, the hitherto known D-A converter has been disadvantageous in that the analog output thereof can not follow up a change or variation in the digital input data at a desirable high speed.

In an attempt to overcome the problem described above, there has been proposed a method according to which the digital input data is divided into a first group of more significant bits and a second group of less significant bits with the first data bit group being processed on the basis of pulse duration modulation (PDM), while the second data bit group is processed through pulse rate modulation (PRM). The processed outputs are then mixed together with each other.

The above method is however disadvantageous in that the circuit arrangement for carrying out the method will become necessarily complicated due to use of both PDM and PRM techniques. Besides, in the case of PRM, the number of pulses to be processed provides a critical problem in addition to the difficulty in attaining a stability of the output pulse due to the inherent pulse rise and fall characteristics of this system, as is known in the art.

Accordingly, an object of the invention is to provide an improved digital-to-analog or D-A converter which is immune to the drawbacks of the hitherto known D-A converter and in which the analog output signal can follow up variations or changes in the input digital data at a high speed.

Another object of the invention is to provide a D-A converter which allows the analog output signal to follow up changes in the digital data input at a high speed by adopting a pulse width modulation principle.

According to the invention there is provided a digital-to-analog converter of the pulse width modulation type comprising a clock pulse generator; a counter of plural-bit capacity coupled to the output of said clock pulse generator for counting the output clock pulses therefrom and for producing a carry signal when the count content of said counter becomes zero; input terminals for the supply of input digital data bits to be converted into an analog signal provided in number corresponding to the bit capacity of said counter; a flip-flop having a set input, a reset input and an output terminal; an integrator connected to the output terminal of said flip-flop for integrating the output signal from said flip-flop; wherein the bits of said counter are classified into two groups of a predetermined number of more significant bits and of the remaining number of less significant bits, while the digital input data bits are classified correspondingly into two groups of a predetermined number of more significant bits and of the remaining number of less significant bits; first means

coupled between said less significant bit terminals of said counter, said digital data input terminals for said more significant bits and said reset input for controlling said flip-flop to divide the counting cycle period of said counter into 2^m elementary sub-periods, where m represents the number of said less significant bits at said digital data input terminals and to allocate a certain number of pulses to each of said elementary sub-periods in dependence on the data value of said more significant bits at said digital data input terminals; and second means connected to the more significant and less significant bit terminals and the carry output terminal of said counter to said digital data input terminals for said less significant bits and to the set input of said flip-flops for controlling the setting of said flip-flop to provide the pulses in said elementary sub-periods under the control of said first means and to provide additional correction elementary pulses to said flip-flop to be allocated to selected ones of said elementary sub-periods in dependence on the data value of said less significant bits of said digital input data.

The following exemplary description teaches that the duration or width of each of the output pulses produced in response to the digital input data in a single counting cycle of a counter and to be subsequently integrated is divided into a number of elementary pulses with the total width thereof being equal to the width of the original pulse. The elementary pulses thus obtained are distributed over a period corresponding to the single counting cycle of the counter thereby to increase the pulse repetition rate or frequency. Thus, the time constant of the succeeding integrator circuit can be made smaller, which in turn allows the analog output to follow up changes in the digital input data more quickly.

In a D-A converter of the PWM type according to an embodiment of the invention, a single counting cycle of the counter is divided into m elementary periods where m represents a preselected number of less significant bits of the digital input data, and the elementary pulses are distributed among the elementary periods in number depending on the logic values of the more significant bits of the digital input data, while supplementary elementary pulses are additionally placed in the elementary periods selectively determined in dependence on the values of the less significant bits of the digital input data.

In this manner, the repetition frequency of the digital output pulses produced during the single counting cycle is virtually converted into the repetition rate of the elementary periods which is 2^m times as high as the former. Thus, the time constant of the succeeding integrator circuit can be made smaller to enhance the response speed of the analog output to the change or variation in the digital input data.

Additionally, since the speed-up of the response of the analog output signal to the variation in the digital input data is effected only on the basis of pulse width modulation, the circuit arrangement can be significantly simplified over the hitherto known converter of the combined PDM and PRM type, while the stability of the pulse which is an advantage of PWM can be effectively retained.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram showing a typical example of hitherto known D-A converters.

Figures 2 and 3 show signal waveform diagrams to illustrate operation of the D-A converter shown in Fig. 1.

Figure 4 is a block diagram showing an exemplary embodiment of the digital-to-analog or D-A converter according to the invention.

Figure 5 shows signal waveform diagram to illustrate operation of the D-A converter shown in Fig. 4.

Figure 6 is a block diagram showing another exemplary embodiment of the D-A converter according to the invention.

Figure 7 shows a signal waveform diagrams to illustrate operation of the D-A converter shown in Fig. 6.

Figure 8 shows signal waveforms of the output signal produced from certain circuits in Figs. 4 and 6.

Figure 9 is a block diagram showing still another embodiment of the D-A converter according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Fig. 4 which is a block diagram showing an exemplary embodiment of a digital-to-analog or D-A converter embodying the present invention, the output of a clock pulse generator 1 is coupled to a counter 2 for counting the clock pulse and having a carry signal output terminal C at which the carry-out signal is produced when the contents of the counter 2 becomes zero or "0". The counter 2 is of for bit capacity, the most significant digit or MSD of which is represented by Q_4 , while the least significant digit or LSD is represented by Q_1 . A digital input signal to be converted into the corresponding analog signal is applied to the digital data input terminals 4a, 4b, 4c and 4d and is composed of four bits, of which MSD is represented by D_4 with LSD being represented by D_1 . Reference numeral 5 denotes a RS flip-flop having a set input S, a reset input R and a Q-output terminal (non-inverted output terminal) to which an integrator circuit 6 is connected for integrating the Q-output (digital value) from the RS flip-flop 5 thereby to produce a corresponding analog value. The analog output from the integrator circuit 6 is connected to a voltage converter 7 having its output con-

nected to a terminal 8 which constitutes the analog output terminal of the D-A converter. A circuit 9 is provided which has first input terminals connected to less significant bit outputs Q_1 and Q_2 of the counter and second input terminals connected to the more significant bit digital data terminals 4d and 4c, while the output of the circuit 9 is connected to the reset input terminal R of the RS flip-flop 5. The circuit 9 serves to divide a single counting cycle or a period of the counter 2 into 2^m elementary periods S_1 to S_4 (refer to Fig. 5) where m represents the number of bits in the less significant bit group 4b; 4a (in the case of the illustrated embodiment, $m = 2$ since there are two elementary bits and thus the number of the elementary periods is equal to 4) and further serves to allocate the pulses in number corresponding to the value of the data bits D_4 and D_3 at the more significant bit input terminals 4d and 4c to each of the elementary periods S_1 to S_4 . The circuit 9 includes a comparator 91 which receives the less significant bits Q_2 ; Q_1 of the counter 2 as first inputs and the more significant bits D_3 ; D_4 from the digital data input terminals 4c and 4d as second inputs thereby to compare the first and second inputs with each other and produce a pulse signal upon coincidence being found in the comparison, which pulse signal is then applied to the reset input terminal R of the flip-flop 5. The broken-line block 10 denotes a correction elementary pulse circuit which has inputs connected to the more significant bit terminals Q_4 ; Q_3 , to the less significant bit terminals Q_2 ; Q_1 and to the carry-out output terminal C of the counter 2 and to the more significant bit terminals 4b; 4a of the digital input terminals. The output from the circuit 10 is connected to the set terminal S of the RS flip-flop 5. The correction elementary pulse circuit 10 serves to allot elementary pulses for correction to selected ones of the elementary periods in dependence on the values of the less significant data bits D_1 ; D_2 of the digital data input terminals. To this end, the circuit 10 includes a comparator circuit 101 having inputs connected to the less significant bit terminals 4b; 4a of the digital data input terminals and to the more significant bit terminals Q_4 ; Q_3 of the counter 2 for the comparison thereof. When coincidence is found between these sets of input bits, the comparator circuit 101 produces a coincidence signal pulse which is then applied to an RS flip-flop 102 at the set terminal S thereof. The RS flip-flop 102 has a reset terminal R connected to the carry-out terminal C of the counter 2. The circuit 10 further includes a comparator 103 which receives the less significant bits Q_2 ; Q_1 of the counter 2 as an input and produces an output signal when these bits all take a certain predetermined value, such as all "1's". This comparator 103 will be thus referred to as the all-"1"-compar-

ator and may be constituted by AND gate 1031. On the other hand, a so-called all-"0"-comparator 104 is provided which has inputs connected to the less significant bits Q_2 and Q_1 and is adapted to produce an output signal when these input bits Q_2 and Q_1 all take a certain predetermined value, such as logic "0". This comparator 104 may be constituted by NOR gate 1041. The circuit 10 further includes an AND gate 105 having inputs connected to the non-inverted or Q-output terminal of the flip-flop 102 and the output terminal of the all-"1"-comparator 103, respectively, and is adapted to produce a number of output pulses in dependence on the less significant bit values D_2 and D_1 at the digital data input terminals 4b and 4a. For example, the AND gate 105 produces a single output pulse when the data bits D_2 and D_1 are all logic "0", two output pulses in response to the logic "0" and "1" of the data bits D_2 and D_1 , three output pulses in response to logic "1" and "0" of data bits D_2 and D_1 , and four output pulses in response to logic "1" and "1" of data bits D_2 and D_1 , respectively. In contrast, there is provided an AND gate 106 which has inputs connected to the inverted or $\bar{Q}$ -output of the flip-flop 102 and the output terminal of the all-"0"-comparator 104 and is adapted to produce a number of output pulses in dependence on the less significant data bits D_2 and D_1 at the digital input terminals 4b and 4a, e.g. four output pulses are produced when data bits D_2 and D_1 are logic "0" and "0", three pulses are produced in response to logic "0" and "1" of data bits D_2 and D_1 , two output pulses are produced in response to logic "1" and "0" of data bits D_2 and D_1 , and a single pulse is produced when data bits D_2 and D_1 are logic "1" and "1", respectively. An OR gate 107 is provided which has input connected to the output terminals of the AND gates 105 and 106, and an output connected to the set input terminal S of the RS flip-flop 5. The outputs from the all-"1"-comparator 103 and the all-"0"-comparator 104 are utilized to define the beginning and the end of the individual elementary period. Of course, other means may be employed to the same effect. The comparator circuit 101 includes a comparator 1015 having first inputs connected to the less significant bit terminals 4b and 4a of the digital data input terminals through inverters 1011 and 1012 for inverting the data bits D_2 and D_1 , respectively, and second inputs connected to the more significant bit terminal Q_4 and Q_3 of the counter 2 for comparing the first and the second input signals with each other, whereby output pulses are produced when coincidence is found in the comparison. For example, when the digital data inputs D_2 and D_1 are "0" and "1", respectively, the comparator 1015 produces output pulses during the times when the more significant bit out-

puts Q_4 and Q_3 of the counter 2 are in the logic states "1" and "0", respectively. The inverters 1011 and 1012 may be alternatively provided between the counter 2 and the comparator 1015. The output of the comparator 1015 is connected to the input of a delay circuit 1016 which serves to delay only the leading edge of the output pulse from the comparator 1015 for a predetermined time (e.g. duration of one clock pulse), thereby to assure that the AND gates 105 and 106 produce the predetermined output pulses without failure. The delay circuit 1016 comprises a D flip-flop having inputs C and D connected to the output of the clock pulse generator 1 and the output of the comparator 1015 and an AND gate 1016' having inputs connected to the Q-output of the D flip-flop 1016 and the output of the comparator 1015. The output of the AND gate 1016' is connected to the set input S of the RS flip-flop 102. In this connection, it should be mentioned that the delay circuitry 1016 is not necessarily required. In practice, if some ripple component is allowable in the output signal from the integrator circuit 6, the delay circuit 1016 may be omitted. Further, although the flip-flop 102 is so connected that it is set by the output from the comparator circuit 101 and reset by the carry-out output from the counter 2, it is also possible to reverse such connection.

Next, operations of the D-A converter shown in Fig. 4 will be described with the aid of signal diagrams shown in Fig. 5, in which output signal waveforms at the main circuit components are illustrated for one count cycle or period of the counter 2 on the assumption that the input digital data D_4 , D_3 , D_2 and D_1 corresponds to "0", "1", "0" and "1", respectively, which represents "5" in decimal notation. In Fig. 5, the clock pulse waveform produced from the clock pulse generator 1 is illustrated at (a), while the digital input data is illustrated at (b). Under these conditions, the all-"1"-comparator 103 and the all-"0"-comparator 104 produce output signals having waveforms illustrated at (c) and (d), respectively, in dependence on whether the less significant bits Q_2 and Q_1 of the counter 2 are simultaneously "1's" or "0's". The comparator 1015 will produce an output signal of the waveform shown at (e) when the more significant bits Q_4 and Q_3 of the counter 2 are logic "1" and "0", respectively, since the less significant data bits D_2 and D_1 at the digital input terminals 4b and 4a are logic "0" and "1" from the above assumption. In response to the output signal of the comparator 1015 and the clock pulse from the clock generator 1 applied to the inputs D and C of the D flip-flop 1016, the latter will produce Q-output (non-inverted output) signal of the waveform shown at (f) in Fig. 5, which is then applied to the AND gate 1016' together with

the output of the comparator 1015 (waveform (e)), resulting in the output signal of the waveform (g) from the AND gate 1016'. the RS flip-flop 102 is set by the output signal (g) from the AND gate 1016' and reset by the carry-out signal of the waveform (h) from the counter 2, thereby to produce output signals of the waveforms shown at (i) and (j) in the set and reset states, respectively. The inverted or Q output (j) from the RS flip-flop 102 is applied to the AND gate 106 together with an output of the wave form (d) from the all-"0"-comparator or NOR gate 104, resulting in the output signal having the waveform shown at (l) from the gate 106 in accordance with the logic values of the less significant bit data D_2 and D_1 of the digital input. On the other hand, AND gate 105 receives at the inputs thereof the output signal (c) from the all-"1"-comparator 103 and the Q-output signal (i) from the RS flip-flop 102, whereby a pulse signal of the waveform shown at (k) in Fig. 5 is produced in accordance with the less significant bit data D_2 and D_1 of the digital input data and is derived as the output signal from the flip-flop 5 to be utilized as the supplementary correction pulse, as described hereinafter. The outputs from AND gates 105 and 106 are input to OR gate 107, resulting in the generation of the logical sum signal of the waveform (m).

On the other hand, the comparator 91 produces a pulse signal in accordance with the more significant data bits D_4 and D_3 at the digital data input terminals 4d and 4c. Since the data bits D_4 and D_3 are logic "0" and "1" from the above assumption, the comparator 91 produces an output signal having waveform shown at (n) in Fig. 5 during the time when the less significant bit output Q_2 and Q_1 of the counter 2 are logic "0" and "1", respectively.

The RS flip-flop 5 is set by the output signal (m) from OR gate 107 and reset by the output signal (n) from the comparator 91, thereby to produce output signal of the waveform shown at (o) in Fig. 5.

In this manner, when the output from the OR gate 107 is utilized as the set signal for the RS flip-flop 5 while the output from the comparator 91 is used as the reset signal, then the output signal pulses from the RS flip-flop 5 will be distributed among the 2^2 elementary or sub-periods S_1 to S_4 (the number of which are determined by the less significant bit number of the digital input data, i.e. two bits D_2 and D_1 at the input terminals 4b and 4a in the illustrated embodiment) as the pulses having durations which in turn depend on the logical values of the more significant data bits D_4 and D_3 . More particularly, when the more significant bits D_4 and D_3 are logic "0" and "1", the distributed pulse has a unit width of an elementary pulse, as indicated by pulses P_1 to P_4 in Fig. 5. When the bits D_4

and D_3 are logic "1" and "0", the distributed pulse will have a pulse width equal to a sum of two elementary pulses. When the bits D_4 and D_3 are both logic "0's", no elementary pulse is present. For the logic states "1" and "1" of the bits D_4 and D_3 , the distributed pulse will have the pulse width equal to a sum of three elementary pulses. The output signals from the RS flip-flop 5 during the elementary or sub-periods S_4 and S_3 are supplementary corrected in dependence on the contents or logic values of the less significant bits by adding the output pulses from the AND gate 105 to the output of gate 106. The distribution of the output pulses described above is determined by the logic values or states of the more significant bits of the digital data input and effected by the output signal from the comparator 91. On the other hand, the supplementary correction of the output signal from the flip-flop 5 depends on the logic value of the less significant bits of the digital data input and effected by the output pulse from the AND gate 105. For example, when the less significant bits D_2 and D_1 are both logic "0's", a single correction pulse is supplemented during the elementary period S_4 . When the bits D_2 and D_1 are logic "0" and "1", two correction pulses P_4' and P_3' are added during the elementary periods S_4 and S_3 , respectively. In the illustrated embodiment, when the less significant bits are logic "0,0"; "0,1"; "1,0" and "1,1", correction pulses are supplementarily allotted to the elementary periods S_4 ; S_4 , S_3 ; S_4 , S_3 , S_2 ; and S_4 , S_3 , S_2 , S_1 , respectively. However, it will be appreciated that such relation may be reversed.

It is to be noted that, when the delay circuit 1016 is omitted, the third pulse P_3 will then be absent in the output signal from RS flip-flop 5, involving a correspondingly increased ripple component.

From the foregoing description, it will be appreciated that the circuit shown in Fig. 4 can produce four output pulses as shown at (o) in Fig. 5 during a single counting cycle of the counter 2 for the digital input data "0101", whereby the pulse repetition frequency is made four times as high as that of the hitherto known circuit which can produce only one output pulse as shown at (d) in Fig. 2 under the same conditions.

By way of example, it is assumed that the four-bit counter is employed in combination with the clock generator producing the clock pulse signal P of 2 MHz. Then, for the digital input data "0101", the output pulse repetition frequency f_1 of the hitherto known system shown in Fig. 1 is calculated as follows:

$$f_1 = \frac{P}{2^4} = \frac{2 \times 10^6}{16} = 125 \text{ KHz}$$

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In contrast, the output pulse repetition frequency f_2 attained in the system according to the invention is equal to 500 KHz as is obvious from the following calculation:

$$f_2 = \frac{P}{2^2} = \frac{2 \times 10^6}{4} = 500 \text{ KHz}$$

This means that the output pulse repetition frequency f_2 attained according to the invention is four times as high as the one attained in the hitherto known circuit such as shown in Fig. 1.

The repetition frequency will vary in dependence on the contents of the digital input data.

The increased pulse repetition frequency will then allow the time constant of the succeeding integrator circuit 6 to be made smaller as compared with the one allowable in the prior art circuit while the ripple component is suppressed within a tolerable range. Thus, it is possible to cause the analog output to follow any variation in the digital input data at a high speed.

The above described embodiment is suited for use in the system in which the digital input data is in a predetermined range of values, e.g. in the range of "0100" to "1011" of the four bit input data. In order to assure a satisfactory operation without erroneous operation in the other ranges of the digital input data such as "0000" to "0011" and "1100" to "1111", that is in the case where the operation is desired over the entire range of the digital input data "0000 - 1111", it is necessary to provide a priority means for selecting with priority either the set input or reset input of the flip-flop 5 as supplied from the outputs of the OR gate 107 and the comparator 91, when both input are produced simultaneously.

Fig. 6 is a circuit diagram showing the D-A converter according to another embodiment of the invention which is different from the one shown in Fig. 4 in that the priority circuit described above is additionally incorporated. In Fig. 6, the like components as those shown in Fig. 4 are denoted by the same reference numerals and the repeated description of such components will be omitted.

Referring to Fig. 6, the priority circuit represented by a broken line block 20 and having inputs connected to the outputs of the circuits 9 and 10 as to the more significant bit terminals 4d and 4c of the digital data input and outputs connected to the set and the reset terminals of the flip-flop 5 will become operative when the digital input data $D_4 - D_1$ at the input terminals 4d to 4a is in the ranges of logic "0000" to "0011" and "1100" to "1111". The priority circuit 20 includes a so-called all-"1"-comparator 201 having inputs connected to the more signifi-

cant bit terminals 4d and 4c, respectively, and adapted to produce an output signal when the more significant input bits D_4 and D_3 take first predetermined logic values such

as all "1's". This comparator 201 may be constituted by an AND gate 2011. On the other hand, an all-"0"-comparator 202 is provided which has inputs connected to the more significant bit input terminals 4d and 4c, respectively, and is adapted to produce an output signal when the more significant bits D_4 and D_3 take second predetermined values such as all "0's". The all-"0"-comparator may be constituted by NOR gate 2021. Additionally, a simultaneous signal detector 203 is provided which has inputs connected to the outputs of the comparator 91 of the first circuit 9 and the OR gate 107 of the second circuit means, respectively, and which is adapted to produce an output signal when the outputs from the comparator 91 and the OR gate 107 are simultaneously produced. The detector 203 may consist of an AND gate 2031, for example. An AND gate 205 is provided which has inputs connected to the output of the detector 203 through an inverter 204 which may consist of an inverter 2041 and is connected to the output of the OR gate 107 of the second circuit means 10, respectively. The priority circuit 20 further includes an AND gate 206 having inputs connected to the outputs of the inverter 204 and the comparator 91 of the first circuit means 9, respectively, an AND gate 207 having inputs connected to the outputs of the all-"1"-comparator 201 and the simultaneous signal generation detector 203, respectively, an AND gate 208 having inputs connected to the outputs of the all-"0"-comparator 202 and the simultaneous signal detector 203, respectively, an OR gate 209 having inputs connected to the outputs of the AND gates 205 and 207, respectively, and an output connected to the set input S of the flip-flop 5, and an OR gate 210 having inputs connected to the outputs of AND gates 206 and 208, respectively, and an output connected to the reset R of the flip-flop 5.

Now, the operation of the priority or preference circuit 20 will be described by referring to Fig. 7 which shows signal waveform diagrams of output signals produced by the main circuit components shown in Fig. 6 during a single counting cycle or period of the counter 2 on the assumption that the input digital data D_4 to D_1 is "0001" ("1" in the decimal notation). Under the stated conditions, the output signal from the all-"1"-comparator 103 and the all-"0"-comparator 104 as well as the carry output signal of the counter 2 have the same respective waveforms as those shown in Fig. 5. Further, since the digital data bits D_2 and D_1 are logic "0" and "1", respectively, the output signal from the comparator 1015 will be of the same waveform as

the one shown in Fig. 5. Consequently, the Q- and $\bar{Q}$ -outputs of the flip-flop 102 as well as the outputs from the AND gates 105 and 106 and the OR gate 107 are also of the same waveform as those shown in Fig. 5. In Fig. 7, the outputs from the AND gates 105 and 106 and the OR gate 107 are shown at (k), (l) and (m), respectively. Because the digital data bits D_4 and D_3 are both "0's", the comparator 91 will produce an output signal having a waveform as shown at (n) in Fig. 7, when the outputs Q_2 and Q_1 of the counter 2 are both "0's". The simultaneous signal detector circuit 203 will produce an output signal having a waveform as shown at (p), when the output of the waveform (m) from OR gate 107 appears simultaneously with the output signal (n) from the comparator 91. The output (p) from the detector circuit 203 is inverted by the inverter 2041 into the waveform shown at (q) in Fig. 7. The AND gate 205 responds then to the output signal (q) of the inverter 2041 and the output signal (m) of OR gate 107 thereby to output a logical product signal having a waveform as shown at (r) in Fig. 7. As will be apparent from the waveform (r), among the output signals from the AND gates 105 and 106 applied to the set input of the RS flip-flop 5, the signal which is produced simultaneously with the output signal from the comparator 91 applied to the reset input R of the flip-flop 5 has been eliminated. Since the digital data bits D_4 and D_3 are both logic "0's" the output of the all-"1"-comparator 201 will be at the logic "0" level, resulting in no output from the AND gate 207. Consequently, the output signal of the waveform (r) from the AND gate 205 will be applied to the set input terminal S of the flip-flop 5 through OR gate 209. Further, the output of the all-"0"-comparator 202 is at the logic level "1" because of the digital bits D_4 and D_3 being both logic "0's". Thus, as the result of the AND function of the gate 208 between the output from the all-"0"-comparator 202 and the output signal (p) from the simultaneous signal detector circuit 203, only one of the reset signal (n) applied to the RS flip-flop 5 that appears in coincidence with the set signal (m) will be produced from the AND gate 208, as is shown at (s) in Fig. 7. Further, through the AND function of the gate 206 between the output signal (n) from the comparator 91 and the output (q), only one of the reset signals (n) that appears out of coincidence with the set signal (m) is produced from the AND gate 206, as is shown at (t) in Fig. 7. The output signals of the OR gates 209 and 210 are illustrated at (u) and (v), respectively, in Fig. 7.

In this manner, the reset signal applied to the RS flip-flop 5 will take the waveform shown at (v) in Fig. 7 and produce an output signal having a waveform as shown at (o) in which A, B and C represent that the reset

signals are selected with preference over the simultaneously produced set signals at these points in time.

In the foregoing description, it has been assumed that the first two more significant bits D_4 and D_3 of the digital input data are both logic "0's". When both of these bits D_4 and D_3 are logic "1's", then the set signal is selected with priority or preference over the reset signal.

In the D-A converter circuit shown in Fig. 6, when the output (m) from the OR gate 107 is not produced simultaneously with the output signal (n) of the comparator 91 (e.g. when the digital input data D_4 to D_1 is "0101"), the simultaneous signal detector circuit 203 remains inoperative. Then, the outputs of AND gates 207 and 208 will be both logic "0's", resulting in the logic "1" output from the inverter 204, whereby the AND gates 205 and 206 are in the conductive state. Consequently, the flip-flop 5 is applied at the set input terminal S with the output signal (m) from the OR gate 107, while the output (n) from the comparator 91 will be applied to the reset input terminal R of the flip-flop 5, which will then produce an output signal having a waveform as shown at (o) in Fig. 5.

In summary, Fig. 8 illustrates waveforms of the Q-output of the RS flip-flop 5 with the digital input data D_4, D_3, D_2, D_1 being increased in the sequence "0000", "0001", "0010", "0011", "0100", "0101", "0110", ..., and "1110" ("0", "1", "2", "3", "4", "5", ..., and "14" in the decimal notation). In Fig. 8, reference letters P_1 to P_4 denote the output pulses distributed among the individual elementary sub-periods S_1 to S_4 through the operation of the first circuit means 9, while P'_1 to P'_4 denotes supplement pulses produced by the second circuit means 10.

Fig. 9 shows a D-A converter incorporating a 12-bit counter to which the invention is applied. The bits Q_1 to Q_{12} of the counter 2 are divided into two groups of eight less significant bits Q_1 to Q_8 and four more significant bits Q_9 to Q_{12} . In this figure, reference numeral 2 denotes the 12-bit counter having the most significant bit or MSB Q_{12} and the least significant bit or LSB Q_1 ; 4a to 4l denotes digital data input terminals for the input data bits having MSB D_{12} and LSB D_1 ; 91 denotes a comparator for comparing the eight less significant bits Q_1 to Q_8 of the counter with the eight more significant data bits D_{12} to D_5 thereby to produce a coincidence output signal when coincidence occurs in the comparison; 101 designates a comparator circuit including a comparator 1015 for comparing the four more significant bit outputs Q_9 to Q_{12} of the counter 2 with four less significant digital input data bits D_4 to D_1 after the digital input data bits D_4 to D_1 having been inverted through respective inverters

1014 to 1011, thereby to produce a coincidence signal upon coincidence occurring in the comparison and a delay circuit 1016 for delay only of the leading edge of the output of the comparator 1015 for a predetermined time (e.g. for a clock pulse duration), the delayed output being supplied to the set input S of a flip-flop 102; reference numeral 103 denotes an all-"1"-comparator for detecting that all of the eight less significant bit outputs Q_1 to Q_8 of the counter 2 become logic "1's"; 104 denotes an all-"0"-comparator for detecting that all of the eight less significant bits Q_1 to Q_8 of the counter 2 become "0's"; 201 denotes an all-"1"-comparator for detecting that all of the eight more significant bits D_{12} to D_5 of the digital input data become logic "1's"; and 202 denotes an all-"0"-comparator for detecting that all of the eight more significant bits D_{12} to D_5 become logic "0's". Since the operations of the above enumerated circuit components are the same as those of the corresponding components shown in Fig. 4, description of the operation will be omitted. Further, the circuit arrangement connected to the outputs of the comparator 91, the RS flip-flop 102, the all-"1"-comparators 103; 201 and the all-"0"-comparators 104; 202 are made in the same manner as in the case of the D-A converter shown in Fig. 6. Therefore, illustration and description thereof will be unnecessary.

In the case of the D-A converter shown in Fig. 9, the single count cycle of the counter 2 is divided into $24 = 16$ elementary or sub-periods with the result that the pulse repetition frequency is about 16-th times as high as that of the hitherto known converter. In more detail, assuming that clock pulse P has frequency of 2 MHz and that a 12-bit counter is employed, then the repetition frequency f_1 in the hitherto known system as shown in Fig. 1 will be:

$$f_1 = \frac{P}{2^{12}} = \frac{2 \times 10^6}{4096} \approx 488.3 \text{ Hz}$$

In contrast, the repetition frequency f_2 of the system shown in Fig. 9 will be:

$$f_2 = \frac{P}{2^8} = \frac{2 \times 10^6}{256} = 7812.5 \text{ Hz}$$

Thus,

$$\frac{f_2}{f_1} = \frac{7812.5}{488.3} \approx 16$$

Such a high repetition frequency permits the time constant to be made even smaller, which in turn increases the response speed of the analog output, while the ripple component

is remarkably reduced in the analog output.

CLAIMS

1. A digital-to-analog converter of the pulse width modulation type comprising a clock pulse generator; a counter of plural-bit capacity coupled to the output of said clock pulse generator for counting the output clock pulses therefrom and for producing a carry signal when the count content of said counter becomes zero; input terminals for the supply of input digital data bits to be converted into an analog signal provided in number corresponding to the bit capacity of said counter; a flip-flop having a set input, a reset input an output terminal; an integrator connected to the output terminal of said flip-flop for integrating the output signal from said flip-flop; wherein the bits of said counter are classified into two groups of a predetermined number of more significant bits and of the remaining number of less significant bits, while the digital input data bits are classified correspondingly into two groups of a predetermined number of more significant bits and of the remaining number of less significant bits; first means coupled between said less significant bit terminals of said counter, said digital data input terminals for said more significant bits and said reset input for controlling said flip-flop to divide the counting cycle period of said counter into 2^m elementary sub-periods, where m represents the number of said less significant bits at said digital data input terminals and to allocate a certain number of pulses to each of said elementary sub-periods in dependence on the data values of said more significant bits at said digital data input terminals; and second means connected to the more significant and less significant bit terminals and the carry output terminal of said counter, to said digital data input terminals for said less significant bits and to the set input of said flip-flop for controlling the setting of said flip-flop to provide the pulses in said elementary sub-periods under the control of said first means and to provide additional correction elementary pulses to said flip-flop to be allocated to selected ones of said elementary sub-periods in dependence on the data value of said less significant bits of said digital input data.
2. A digital-to-analog converter as set forth in claim 1, including preference means coupled between the outputs of said first and second means, said digital data input terminals for said more significant bits and the set and the reset inputs of said flip-flop for supplying the outputs of said first and second means to the set and reset inputs of said flip-flop, wherein said preference means is adapted to select either one of said outputs of said first and second means in dependence on the data value of said more significant bits at said digital data input terminals when both of said outputs are simultaneously produced



1014 to 1011, thereby to produce a coincidence signal upon coincidence occurring in the comparison and a delay circuit 1016 for delay only of the leading edge of the output of the comparator 1015 for a predetermined time (e.g. for a clock pulse duration), the delayed output being supplied to the set input S of a flip-flop 102; reference numeral 103 denotes an all-'1'-comparator for detecting that all of the eight less significant bit outputs Q_1 to Q_8 of the counter 2 become logic '1's'; 104 denotes an all-'0'-comparator for detecting that all of the eight less significant bits Q_1 to Q_8 of the counter 2 become '0's'; 201 denotes an all-'1'-comparator for detecting that all of the eight more significant bits D_{12} to D_5 of the digital input data become logic '1's'; and 202 denotes an all-'0'-comparator for detecting that all of the eight more significant bits D_{12} to D_5 become logic '0's'. Since the operations of the above enumerated circuit components are the same as those of the corresponding components shown in Fig. 4, description of the operation will be omitted. Further, the circuit arrangement connected to the outputs of the comparator 91, the RS flip-flop 102, the all-'1'-comparators 103; 201 and the all-'0'-comparators 104; 202 are made in the same manner as in the case of the D-A converter shown in Fig. 6. Therefore, illustration and description thereof will be unnecessary.

In the case of the D-A converter shown in Fig. 9, the single count cycle of the counter 2 is divided into $24 = 16$ elementary or sub-periods with the result that the pulse repetition frequency is about 16-th times as high as that of the hitherto known converter. In more detail, assuming that clock pulse P has frequency of 2 MHz and that a 12-bit counter is employed, then the repetition frequency f_1 in the hitherto known system as shown in Fig. 1 will be:

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Thus,

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Such a high repetition frequency permits the time constant to be made even smaller, which in turn increases the response speed of the analog output, while the ripple component

is remarkably reduced in the analog output.

CLAIMS

1. A digital-to-analog converter of the pulse width modulation type comprising a clock pulse generator; a counter of plural-bit capacity coupled to the output of said clock pulse generator for counting the output clock pulses therefrom and for producing a carry signal when the count content of said counter becomes zero; input terminals for the supply of input digital data bits to be converted into an analog signal provided in number corresponding to the bit capacity of said counter; a flip-flop having a set input, a reset input an output terminal; an integrator connected to the output terminal of said flip-flop for integrating the output signal from said flip-flop; wherein the bits of said counter are classified into two groups of a predetermined number of more significant bits and of the remaining number of less significant bits, while the digital input data bits are classified correspondingly into two groups of a predetermined number of more significant bits and of the remaining number of less significant bits; first means coupled between said less significant bit terminals of said counter, said digital data input terminals for said more significant bits and said reset input for controlling said flip-flop to divide the counting cycle period of said counter into 2^m elementary sub-periods, where m represents the number of said less significant bits at said digital data input terminals and to allocate a certain number of pulses to each of said elementary sub-periods in dependence on the data values of said more significant bits at said digital data input terminals; and second means connected to the more significant and less significant bit terminals and the carry output terminal of said counter, to said digital data input terminals for said less significant bits and to the set input of said flip-flop for controlling the setting of said flip-flop to provide the pulses in said elementary sub-periods under the control of said first means and to provide additional correction elementary pulses to said flip-flop to be allocated to selected ones of said elementary sub-periods in dependence on the data value of said less significant bits of said digital input data.

2. A digital-to-analog converter as set forth in claim 1, including preference means coupled between the outputs of said first and second means, said digital data input terminals for said more significant bits and the set and the reset inputs of said flip-flop for supplying the outputs of said first and second means to the set and reset inputs of said flip-flop, wherein said preference means is adapted to select either one of said outputs of said first and second means in dependence on the data value of said more significant bits at said digital data input terminals when both of said outputs are simultaneously produced



from said first and second means thereby to supply the selected one of said outputs to said flip-flop.

3. A digital-to-analog converter as set forth in Claim 1 or 2, wherein said first means includes first comparator means coupled between said digital data input terminals for said more significant bits, the less significant bit terminals of said counter and the reset input terminal of said flip-flop for comparing said more significant bits of said digital input data with said less significant bits of said counter thereby to produce an output signal upon coincidence being found in said comparison, said output signal being applied to said reset input of said flip-flop; and wherein said second means includes second comparator means coupled between said digital data input terminals for said less significant bits and the more significant bit terminals of said counter for comparing said less significant bits of said digital input data with said more significant bits of said counter thereby to produce an output signal upon coincidence being found in said comparison; a second flip-flop coupled between the output of said second comparator means and said carry output terminal of said counter and adapted to be set and reset by the output from said second comparator means and said carry output of said counter; third comparator means coupled to the less significant bit terminals of said counter for producing an output signal when said less significant bits of said counter take first predetermined values, fourth comparator means coupled to said less significant bit terminals of said counter for producing an output signal when said less significant bits of said counter take second pre-determined values; and circuit means coupled to a non-inverted output and an inverted output of said second flip-flop, the outputs of said third and fourth comparator means and said set input terminal of said flip-flop for producing a logical product from said non-inverted output of said second flip-flop and the output of said third comparator means as well as a logical product from said inverted output of said second flip-flop and the output of said fourth comparator means, said logical product signals being supplied to the set input of said flip-flop.

4. A digital-to-analog converter as set forth in Claim 3, wherein said second comparator means includes inverter means coupled to said digital data input terminals for said less significant bits thereby to invert the values of said less significant bits; and a comparator coupled to the inverted output of said inverter means and said more significant bits of said counter for comparing said inverted output with said more significant bits of said counter thereby to produce an output signal upon coincidence being found in said comparison.

5. A digital-to-analog converter as set forth in Claim 4, wherein delay means is provided for delaying only the leading edge of said output signal from said comparator for a duration corresponding to a predetermined number of clock pulses.

6. A digital-to-analog converter as set forth in Claim 3, 4 or 5, wherein said third comparator means includes a first comparator for producing an output signal in response to all of said less significant bits of said counter being logic "1's", and wherein said fourth comparator means includes a second comparator for producing an output signal in response to all of said less significant bits of said counter being logic "0's".

7. A digital-to-analog converter as set forth in Claim 6, wherein said delay means includes a D flip-flop coupled to said clock pulse generator circuit and said second comparator for receiving outputs therefrom, and an AND circuit coupled to said D flip-flop and said second comparator for producing a logical product of the outputs therefrom, thereby to delay only the leading edge of the output from said second comparator for a duration corresponding to a predetermined number of clock pulses.

8. A digital-to-analog converter as set forth in any one of Claims 3 to 7, wherein the first predetermined values are logic "1's" and the second predetermined values are logic "0's".

9. A digital-to-analog converter as set forth in Claim 8, wherein said third comparator means includes a first AND circuit while said fourth comparator means includes a NOR circuit, and wherein said circuit means includes a second AND circuit coupled to the output of said first AND circuit and the non-inverted output of said second flip-flop thereby to produce a logical product thereof; a third AND circuit coupled to the output of said NOR circuit and the inverted output of said second flip-flop thereby to produce a logical product thereof, and an OR circuit coupled to the outputs of said second and third AND circuits and the set input of said first flip-flop for producing a logical sum from the outputs of said second and third AND circuits to be supplied to said set input of said first flip-flop.

10. A digital-to-analog converter as set forth in Claim 2, wherein said preference circuit means comprises first comparator means coupled to said digital data input terminals for said more significant bits for producing an output signal when said more significant bits take first predetermined values; a second comparator means coupled to said digital data input terminals for said more significant bits for producing an output signal when said more significant bits take second predetermined values; simultaneous signal detector circuitry coupled to the outputs of said first and second means for producing an out-



put signal corresponding to a logical product of the output signals from said first and second means when both of said output signals are produced simultaneously; inverter means for inverting the output signal of said detector circuitry; first circuit means coupled to the outputs of said inverter means and said second means for producing a logical product of said outputs; second circuit means coupled to the output of said inverter means and said first means for producing a logical product of said outputs; third circuit means coupled to the outputs of said first comparator means and said simultaneous signal detector circuitry for producing a logical product of said outputs; fourth circuit means coupled to the outputs of said second comparator means and said simultaneous signal detector circuitry for producing a logical product of said outputs, fifth circuit means coupled to the outputs of said first and third circuit means and the set input of flip-flop for producing a logical sum of said outputs of said first and third circuit means, said logical sum signal being supplied to the set input of said flip-flop; and sixth circuit means coupled to the outputs of said second and fourth circuit means and the reset input of said flip-flop for producing a logical sum of said outputs from said second and fourth circuit means, said logical sum signal being supplied to the reset input of said flip-flop.

11. A digital-to-analog converter as set forth in Claim 8 or 9, including fifth comparator means coupled to said digital data input terminals for said more significant bits for producing an output signal when said more significant bits take first predetermined values; sixth comparator means coupled to said digital data input terminals for said more significant bits for producing an output signal when said more significant bits take second predetermined values; a simultaneous signal detector circuit coupled to the outputs of said first comparator and said circuit means for producing an output signal corresponding to a logical product of the output signals from said first comparator and said circuit means when both of said output signals are produced simultaneously; inverter means for inverting the output signal of said detector circuit; second circuit means coupled to the outputs of said inverter means and said circuit means for producing a logical product of said outputs; third circuit means coupled to the output of said inverter means and said first comparator for producing a logical product of said outputs; fourth circuit means coupled to the outputs of said fifth comparator means and said simultaneous signal detector circuit for producing a logical product of said outputs; fifth circuit means coupled to the outputs of said sixth comparator means and said simultaneous signal detector circuit for producing a logical product of said outputs, sixth circuit means coupled to

the outputs of said second and fourth circuit means for producing a logical sum of said outputs of said second and fourth circuit means; seventh circuit means coupled to the outputs of said third and fifth circuit means for producing a logical sum of said outputs from said third and fifth circuit means, the first flip-flop being coupled to the outputs of said sixth and seventh circuit means to be set and reset by said sixth and seventh circuit means.

11. A digital-to-analog converter constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figs. 4 to 9 of the accompanying drawings.

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