# INTEGRATED VCSELs ON TRADITIONAL VLSI PACKAGING

## FIELD OF THE INVENTION

**[0001]** The present invention is related generally to the field of integrated circuit modules and more specifically to the field of integrated circuit modules including vertical cavity surface-emitting lasers.

## BACKGROUND OF THE INVENTION

**[0002]** Vertical Cavity Surface Emitting Laser (VCSEL) arrays are often used in fiber optic communications. These VCSEL arrays are capable of transmitting large amounts of data over small optical fibers. A single 1/8 inch fiber bundle may carry an entire 12-20 bit logical port running at relatively high speeds. VCSEL arrays are constructed using semiconductor process techniques similar to those used in silicon integrated circuits, however, the process techniques used for VCSEL arrays may not be optimal for construction of high speed silicon integrated circuits. This makes it difficult to integrate VCSEL arrays and high speed circuits on the same silicon device.

**[0003]** Many current uses of VCSEL technology require precise performance specifications in order to transmit signals over long distances via optical fibers. However, in situations where only short distances are required, such as within a computer server or within a single data center, less stringent performance specifications are required of the VCSEL arrays.

**[0004]** Currently, some circuit boards include VCSEL array modules and receiver modules for communication between computers. Typically, these modules are placed along one edge of the board and electrically connected to one or more electronic

devices attached to the board. These solutions work well, however as computer speeds continue to increase, the delay inherent in driving signals out of an electronic device, into a board, along a board electrical connector, and into a VCSEL array module becomes increasingly troublesome to engineers designing high-speed computers.

**[0005]** Further, board space may be very expensive and in short supply especially in devices such as desktop systems or blade servers. The footprint of separate VCSEL array modules and, if needed, their translator/terminator devices may become a substantial portion of total board area, thus increasing size and costs of the computer.

## SUMMARY OF THE INVENTION

**[0006]** A circuit module including at least one Application Specific Integrated Circuit (ASIC) and a plurality of Vertical Cavity Surface-Emitting Laser (VCSEL) array modules is built using a standard ceramic or organic VLSI package substrate, resulting is a high density device with a small footprint. Interconnection between the electronic devices and the VCSEL array modules is accomplished using standard integrated circuit packaging technology and flexible connectors. Optical connections from the VCSEL arrays to fiber optic cables are made possible by integrating industry-standard optical connectors onto the package. Optical receiver and transceiver modules may also be incorporated into the circuit module.

**[0007]** Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is a top view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention.

[0009] Figure 2 is a top view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention.

[0010] Figure 3A is a cross-sectional view of an example embodiment of a prior art circuit module connecting to an external VCSEL.

[0011] Figure 3B is a cross-sectional view of the external VCSEL shown in Figure 2A.

[0012] Figure 4 is a top view of an example embodiment of a VLSI circuit module before attachment of a plurality of integrated VCSEL array modules according to the present invention.

[0013] Figure 5A is a cross-sectional view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention.

[0014] Figure 5B is a cross-sectional view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention.

[0015] Figure 6 is a top view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention.

[0016] Figure 7 is a top view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention.

[0017] Figure 8 is a flowchart representing a method for the construction of a VLSI circuit module a plurality of including integrated VCSEL array modules according to the present invention.

[0018] Figure 9 is a top view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention.

[0019] Figure 10 is a top view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention.

[0020] Figure 11 is a flowchart representing a method for the construction of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention.

## DETAILED DESCRIPTION

[0021] Figure 1 is a top view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention. A standard VLSI package substrate **100** constructed of a common package material, such as a ceramic or organic material, is shown in this example embodiment of the present invention with a single large application specific integrated circuit (ASIC) **102** attached to the substrate **100** underneath a standard heat spreader **114**. Another invention including integrated VCSELs is described in a U.S. patent application, Serial No. _____, "Circuit Module Including Integrated VCSELs", filed on December 12, 2002, and incorporated herein by reference. Another invention including VCSELs on ASIC substrates is described in a U.S. patent application, Serial No. _____, "Integrated VCSELs on ASIC Module Using Flexible Electrical

Connections", filed concurrently with the present application, and incorporated herein by reference. The ASIC **102** may be any one of a number of integrated circuit devices, such as a microprocessor, memory, cross-bar, cache controller, FPGA, or any of a number of large scale integrated (LSI) or very large scale integrated (VLSI) circuits. Also present on the substrate are a quantity of VCSEL array modules **106**, receivers **108**, and transceivers **110**. Signal ports **112** connect the ASIC **102** to the VCSEL array modules **106**, receivers **108**, and the transceivers **110** through small flexible connectors **104**. The small flexible connectors **104** allow a 90-degree transition in signal direction in an electrical rather than an optical path resulting in less complexity and ease of manufacturing. Since the light beam from a VCSEL is emitted perpendicular to the surface of the VCSEL, when a VCSEL is attached to the flexible connector **104** which includes a 90-degree bend, the VCSEL itself is now perpendicular to the plane of the ASIC substrate **100** and the light from the VCSEL is emitted in a plane parallel to that of the ASIC substrate **100**. The plurality of signal lines connecting the ASIC **102** to the signal ports **112** within the substrate **100** are not shown in this figure for clarity reasons. In an example embodiment of the present invention the VCSEL array modules **106** may incorporate industry standard optical connectors into the module allowing optical connection from the VCSEL array modules **106** using industry standard connections. In this example embodiment of the present invention, the VCSEL circuit is perpendicular to the plane of the substrate **100** and the industry standard connectors are attached such that light is transmitted in a plane parallel to that of the substrate **100**. Note that this example embodiment shows a total of 16 VCSEL array modules **106**, receivers **108** and transceivers **110**. Those of skill in the art will recognize that any number and any combination of VCSEL array

modules **106**, receivers **108**, and transceivers **110** may be used within the scope of the present invention.

**[0022]** Figure 2 is a top view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention. The example embodiment of the present invention shown in Figure 2 is similar to that of Figure 1 with the exception that instead of a single ASIC **102** attached to a substrate **100**, a first ASIC **202**, a second ASIC **204**, a third ASIC **206**, and a fourth ASIC **208** are attached to the substrate **200**. Also, Figure 2 does not include a heat spreader so that the individual ASICs and their interconnections are visible. Signal ports **212** connect the ASICs **202**, **204**, **206**, and **208** to the VCSEL array modules **216**, receivers **218**, and the transceivers **220** through small flexible connectors **214**. The small flexible connectors **214** allow a 90-degree transition in signal direction in an electrical rather than an optical path resulting in less complexity and ease of manufacturing. The plurality of signal lines connecting the ASICs **202**, **204**, **206**, and **208** to the signal ports **212** within the substrate **200** are not shown in this figure for clarity reasons. In an example embodiment of the present invention the VCSEL array modules **216** may incorporate industry standard optical connectors into the module allowing optical connection from the VCSEL array modules **216** using industry standard connections. Similar to Figure 1, in this example embodiment of the present invention, the VCSEL circuit is perpendicular to the plane of the substrate **200** and the industry standard connectors are attached such that light is transmitted in a plane parallel to that of the substrate **200**. Note that this example embodiment shows a total of 16 VCSEL array modules **216**, receivers **218** and transceivers **220**. Those of skill in the art will recognize that any number and any combination of VCSEL array modules **216**, receivers **218**, and transceivers **220** may be used within

the scope of the present invention. Also present in this example embodiment of the present invention are a plurality of signal lines **210** electrically connecting the four ASICs **202, 204, 206,** and **208** to each other.

**[0023]** Figure 3A is a cross-sectional view of an example embodiment of a prior art circuit module connecting to an external VCSEL. An electronic device **306** is shown attached to a first package **302** through a C4 attach bump **308**. Within the first package **302**, a package trace **310** electrically connects the electronic device **306** to a first ball grid array (BGA) ball **312**. This first BGA ball **312** electrically connects the first package **302** to a board **300**. Within the board **300**, a first board via **314** electrically connects the BGA ball **312** to a board trace **316**, and through the board trace **316** to a second board via **318**. This second board via **318** is electrically coupled to a second BGA ball **320** attached to a second package **304** containing a VCSEL.

**[0024]** Figure 3B is a cross-sectional view of the external VCSEL shown in Figure 3A. Within the second package **304** a second package via **326** electrically couples the second BGA ball **320** to a package pad **328**, which is in turn electrically connected to a VCSEL **332** through a second package trace **330** and a flexible electrical conductor **334**. The VCSEL **332** is then optically coupled to an industry standard optical connector **322**. Note that in this example embodiment of a VCSEL module, the VCSEL **332** is configured perpendicular to the board **300**. Thus the light emitted from the VCSEL is in a plane parallel to the board **300** and the industry standard optical connector **322** is configured to route any optical conductors in a plane parallel to the board **300**.

**[0025]** Figure 4 is a top view of an example embodiment of a VLSI circuit module substrate before attachment of a plurality of integrated VCSEL array modules according to the present invention. A standard VLSI circuit substrate **400** is shown

including a cavity **402** and a plurality of signal ports **404**. Within the cavity **402** are a plurality of VLSI signal ports **406** that are electrically connected to the signal ports **404** through conductors within the substrate **400**. These conductors are not shown in this figure for clarity.

**[0026]** Figure 5A is a cross-sectional view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention. A substrate **500** is shown including a cavity **506**. Those of skill in the art will recognize that alternate package and heat spreader arrangements without a cavity may be used within the scope of the present invention. Within the cavity **506** is an ASIC **504** electrically connected to VLSI signal ports **508** on the substrate **500**. A heat spreader **502** is thermally coupled to the ASIC and mechanically coupled to the substrate **500** sealing the cavity **506**. ASIC signal lines **512** run through the substrate **500** to standard package pads **510**. Those of skill in the art will recognize that these package pads **510** may be constructed in a wide variety of styles and configurations within the scope of the present invention. For example, the package may be a ball grid array (BGA) package and the package pads **510** would then comprise individual solder balls. VCSEL signal lines **514** run through the substrate **500** to VCSEL signal ports **516**. A VCSEL array **522** is electrically connected to the VCSEL signal ports **516**. Note that in this example embodiment of the present invention, the VCSEL array **522** is in a plane parallel to that of the substrate **500** and the light emitted from the VCSEL array **522** is in a plane perpendicular to that of the substrate **500**.

**[0027]** Figure 5B is a cross-sectional view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention. Figure 5B is identical to Figure 5A with the exception that the VCSEL array is attached to the substrate **500** through a flexible connector **518** rather

than directly. A substrate **500** is shown including a cavity **506**. Those of skill in the art will recognize that alternate package and heat spreader arrangements without a cavity may be used within the scope of the present invention. Within the cavity **506** is an ASIC **504** electrically connected to VLSI signal ports **508** on the substrate **500**. A heat spreader **502** is thermally coupled to the ASIC and mechanically coupled to the substrate **500** sealing the cavity **506**. ASIC signal lines **512** run through the substrate **500** to standard package pads **510**. Those of skill in the art will recognize that these package pads **510** may be constructed in a wide variety of styles and configurations within the scope of the present invention. For example, the package may be a ball grid array (BGA) package and the package pads **510** would then comprise individual solder balls. VCSEL signal lines **514** run through the substrate **500** to VCSEL signal ports **516**. A VCSEL array **520** is electrically connected to the VCSEL signal ports **516** through a small flexible circuit board **518**. Since the light beam from a VCSEL is emitted perpendicular to the surface of the VCSEL, when a VCSEL is attached to the flexible circuit board **518** which includes a 90-degree bend, the VCSEL itself is now perpendicular to the plane of the substrate **500** and the light from the VCSEL is emitted in a plane parallel to that of the substrate **500**. The small flexible circuit board **518** contains electrical traces configured to connect the VCSEL array **520** to the VCSEL signal ports **516**.

**[0028]** Figure 6 is a top view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention. A standard VLSI package substrate **600** constructed of a common package material, such as a ceramic or organic material, is shown in this example embodiment of the present invention with a single large application specific integrated circuit (ASIC) **602** attached to the substrate **600** underneath a standard heat spreader **614**.

The ASIC **602** may be any one of a number of integrated circuit devices, such as a microprocessor, memory, cross-bar, cache controller, FPGA, or any of a number of large scale integrated (LSI) or very large scale integrated (VLSI) circuits. Also present on the substrate are a quantity of VCSEL array modules **606**, receivers **608**, and transceivers **610**. Signal ports **604** connect the ASIC **602** to the VCSEL array modules **606**, receivers **608**, and the transceivers **610** through a single large flexible connector **612**. The plurality of signal lines connecting the ASIC **602** to the signal ports **604** within the substrate **600** are not shown in this figure for clarity reasons. In an example embodiment of the present invention the VCSEL array modules **606** may incorporate industry standard optical connectors into the module allowing optical connection from the VCSEL array modules **606** using industry standard connections. In this example embodiment of the present invention, the VCSEL circuit is perpendicular to the plane of the substrate **600** and the industry standard connectors are attached such that light is transmitted in a plane parallel to that of the substrate **600**. Note that this example embodiment shows a total of 16 VCSEL array modules **606**, receivers **608** and transceivers **610**. Those of skill in the art will recognize that any number and any combination of VCSEL array modules **606**, receivers **608**, and transceivers **610** may be used within the scope of the present invention.

**[0029]** Figure 7 is a top view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention. Figure 7 is identical to Figure 6 with the exception that a plurality of terminators, translators, or other components are attached to the flexible connector. A standard VLSI package substrate **700** constructed of a common package material, such as a ceramic or organic material, is shown in this example embodiment of the present invention with a single large application specific integrated circuit (ASIC) **702**

attached to the substrate **700** underneath a standard heat spreader **716**. The ASIC **702** may be any one of a number of integrated circuit devices, such as a microprocessor, memory, cross-bar, cache controller, FPGA, or any of a number of large scale integrated (LSI) or very large scale integrated (VLSI) circuits. Also present on the substrate are a quantity of VCSEL array modules **706**, receivers **708**, and transceivers **710**. Signal ports **704** connect the ASIC **702** to the VCSEL array modules **706**, receivers **708**, and the transceivers **710** through a single large flexible connector **714**. Also present on the large flexible connector **714** are a plurality of components **712** such as terminators or translators as needed between the ASIC **702** and the VCSEL array modules **706**. The plurality of signal lines connecting the ASIC **702** to the signal ports **704** within the substrate **700** are not shown in this figure for clarity reasons. In an example embodiment of the present invention the VCSEL array modules **706** may incorporate industry standard optical connectors into the module allowing optical connection from the VCSEL array modules **706** using industry standard connections. In this example embodiment of the present invention, the VCSEL circuit is perpendicular to the plane of the substrate **700** and the industry standard connectors are attached such that light is transmitted in a plane parallel to that of the substrate **700**. Note that this example embodiment shows a total of 16 VCSEL array modules **706**, receivers **708** and transceivers **710**. Those of skill in the art will recognize that any number and any combination of VCSEL array modules **706**, receivers **708**, and transceivers **710** may be used within the scope of the present invention.

**[0030]** Figure 8 is a flowchart representing a method for the construction of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention. In a step **800** a VLSI package substrate is provided. In a step

802 at least one ASIC is attached to the substrate. In a decision step 804 if VCSEL array modules are to be used, control is passed to step 806, if not, control is passed to step 810. In a step 806, a plurality of VCSEL array modules are attached to a flexible connector. In a step 808, the VCSEL array modules are electrically connected to the ASICs through the flexible connector. In a decision step 810 if VCSEL transceiver modules are to be used, control is passed to step 812, if not, control is passed to step 816. In a step 812 a plurality of VCSEL transceiver modules are attached to a flexible connector. In a step 814 the VCSEL transceiver modules are electrically connected to the ASICs through the flexible connector. In a decision step 816 if optical receiver modules are to be used, control is passed to step 818, if not, control is passed to step 822. In a step 818 a plurality of optical receiver modules are attached to a flexible connector. In a step 820 the optical receiver modules are electrically connected to the ASICs through the flexible connector. In a decision step 822 if a heat spreader is to be added to the module, control is passed to step 824, if not, control is passed to the end step 826. In a step 824 a heat spreader is mechanically attached to the substrate such that it is thermally coupled to at least one ASIC. Those of skill in the art will recognize that the steps in this method may be performed in a very wide variety of different orders within the scope of the present invention.

[0031] Figure 9 is a top view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention. A standard VLSI package substrate 900 constructed of a common package material, such as a ceramic or organic material, is shown in this example embodiment of the present invention with a single large application specific integrated circuit (ASIC) 902 attached to the substrate 900 underneath a standard heat spreader 904. The ASIC 902 may be any one of a number of integrated circuit devices, such as a

microprocessor, memory, cross-bar, cache controller, FPGA, or any of a number of large scale integrated (LSI) or very large scale integrated (VLSI) circuits. Also present on the substrate are a quantity of VCSEL array modules **906**, receivers **908**, and transceivers **910**. Note that in this example embodiment of the present invention the VCSEL array modules **906**, receivers **908**, and transceivers **910** are attached directly to the VLSI package substrate in a vertical configuration through a plurality of signal ports. The plurality of signal lines connecting the ASIC **902** to signal ports within the substrate **900** are not shown in this figure for clarity reasons. In an example embodiment of the present invention the VCSEL array modules **906** may incorporate industry standard optical connectors into the module allowing optical connection from the VCSEL array modules **906** using industry standard connections. In this example embodiment of the present invention the VCSEL array modules **906** are configured in a plane parallel to that of the substrate **900**. The light emitted from the VCSEL array modules **906** will be in a plane perpendicular to that of the substrate **900**, and any industry standard connections attached to the VCSEL arrays will be in a vertical configuration. Note that this example embodiment shows a total of 16 VCSEL array modules **906**, receivers **908** and transceivers **910**. Those of skill in the art will recognize that any number and any combination of VCSEL array modules **906**, receivers **908**, and transceivers **910** may be used within the scope of the present invention.

**[0032]** Figure 10 is a top view of an example embodiment of a VLSI circuit module including a plurality of integrated VCSEL array modules according to the present invention. Figure 10 is identical to Figure 9 with the exception that the VCSEL array modules **1006**, receivers **1008**, and transceivers **1010** are attached to the substrate in a horizontal configuration. A standard VLSI package substrate **1000** constructed of a

common package material, such as a ceramic or organic material, is shown in this example embodiment of the present invention with a single large application specific integrated circuit (ASIC) **1002** attached to the substrate **1000** underneath a standard heat spreader **1004**. The ASIC **1002** may be any one of a number of integrated circuit devices, such as a microprocessor, memory, cross-bar, cache controller, FPGA, or any of a number of large scale integrated (LSI) or very large scale integrated (VLSI) circuits. Also present on the substrate are a quantity of VCSEL array modules **1006**, receivers **1008**, and transceivers **1010**. Note that in this example embodiment of the present invention the VCSEL array modules **1006**, receivers **1008**, and transceivers **1010** are attached directly to the VLSI package substrate **1000** in a plane parallel to that of the substrate **1000** through a plurality of signal ports. The plurality of signal lines connecting the ASIC **1002** to signal ports within the substrate **1000** are not shown in this figure for clarity reasons. In an example embodiment of the present invention the VCSEL array modules **1006** may incorporate industry standard optical connectors into the module allowing optical connection from the VCSEL array modules **1006** using industry standard connections. The light emitted from the VCSEL array modules **1006** will be in a plane perpendicular to that of the substrate **1000**, and any industry standard connections attached to the VCSEL arrays will be in a vertical configuration. Note that this example embodiment shows a total of 16 VCSEL array modules **1006**, receivers **1008** and transceivers **1010**. Those of skill in the art will recognize that any number and any combination of VCSEL array modules **1006**, receivers **1008**, and transceivers **1010** may be used within the scope of the present invention.

**[0033]** Figure 11 is a flowchart representing a method for the construction of a VLSI circuit module including a plurality of integrated VCSEL array modules according to

the present invention. The method shown in Figure 11 is identical to the method shown in Figure 8 with the exception that the VCSEL modules are directly attached to the VLSI package substrate instead of being attached through a flexible connector. In a step **1100** a VLSI package substrate is provided. In a step **1102** at least one ASIC is attached to the VLSI package substrate. In a decision step **1104** if VCSEL array modules are to be used, control is passed to step **1106**, if not, control is passed to step **1110**. In a step **1106**, a plurality of VCSEL array modules are attached to the VLSI package substrate. In a step **1108**, the VCSEL array modules are electrically connected to the ASICs through the VLSI package substrate. In a decision step **1110** if VCSEL transceiver modules are to be used, control is passed to step **1112**, if not, control is passed to step **1116**. In a step **1112** a plurality of VCSEL transceiver modules are attached to the VLSI package substrate. In a step **1114** the VCSEL transceiver modules are electrically connected to the ASICs through the VLSI package substrate. In a decision step **1116** if optical receiver modules are to be used, control is passed to step **1118**, if not, control is passed to step **1122**. In a step **1118** a plurality of optical receiver modules are attached to the VLSI package substrate. In a step **1120** the optical receiver modules are electrically connected to the ASICs through the VLSI package substrate. In a decision step **1122** if a heat spreader is to be added to the module, control is passed to step **1124**, if not, control is passed to the end step **1126**. In a step **1124** a heat spreader is mechanically attached to the substrate such that it is thermally coupled to at least one ASIC. Those of skill in the art will recognize that the steps in this method may be performed in a very wide variety of different orders within the scope of the present invention.

**[0034]** The foregoing description of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit

the invention to the precise form disclosed, and other modifications and variations may be possible in light of the above teachings. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application to thereby enable others skilled in the art to best utilize the invention in various embodiments and various modifications as are suited to the particular use contemplated. It is intended that the appended claims be construed to include other alternative embodiments of the invention except insofar as limited by the prior art.

FOREIGN CLAIMS

What is claimed is:

1. A circuit module comprising:

a VLSI package substrate **500**;

an ASIC **504** attached to said VLSI package substrate **500**; and

a plurality of VCSEL array modules **522** attached to said VLSI package substrate **500** and electrically coupled to said ASIC **504** through said VLSI package substrate **500**.

2. A circuit module comprising:

a VLSI package substrate **500**;

an ASIC **504** attached to said VLSI package substrate **500**;

at least one flexible connector **518** attached to said VLSI package substrate **500** and electrically coupled to said ASIC **504**; and

a plurality of VCSEL array modules **520** attached to said at least one flexible connector **518** and electrically coupled to said ASIC **504** through said at least one flexible connector **518**.

3. A circuit module comprising:

a VLSI package substrate **500**;

an ASIC **504** attached to said VLSI package substrate **500**; and

a plurality of optical receiver modules **522** attached to said VLSI package substrate **500** and electrically coupled to said ASIC **504** through said VLSI package substrate **500**.

4. A circuit module comprising:

a VLSI package substrate **500**;

an ASIC **504** attached to said VLSI package substrate **500**;

at least one flexible connector **518** attached to said VLSI package substrate **500** and electrically coupled to said ASIC **504**; and

a plurality of optical receiver modules **520** attached to said at least one flexible connector **518** and electrically coupled to said ASIC **514** through said at least one flexible connector **518**.

5. A circuit module comprising:

a VLSI package substrate **500**;

an ASIC **504** attached to said VLSI package substrate **500**; and

a plurality of VCSEL transceiver modules **522** attached to VLSI package substrate **500** and electrically coupled to said ASIC **504** through said VLSI package substrate **500**.

6. A circuit module comprising:

a VLSI package substrate **500**;

an ASIC **504** attached to said VLSI package substrate **500**;

at least one flexible connector **518** attached to said VLSI package substrate **500** and electrically coupled to said ASIC **504**; and

a plurality of VCSEL transceiver modules **520** attached to said at least one flexible connector **518** and electrically coupled to said ASIC **504** through said at least one flexible connector **518**.