CLAIMS

1. A bit interleaving method interleaving a codeword of quasi-cyclic low-density parity check codes, including repeat-accumulate quasi-cyclic low-density parity check codes,

the bit interleaving method comprising:

an allocation step of allocating codeword bits of the codeword made up of N cyclic blocks each including Q bits to $Q \times N/M$ constellation words, each of the constellation words being made up of M bits, wherein

N is a multiple of M/F,

F is an integer greater than one, and is a divisor of M and Q, and

in the allocation step, the M bits in each of the Q/F constellation words include F bits from each of M/F different cyclic blocks in $F \times N/M$ folding sections each made up of M/F cyclic blocks.

2. A bit interleaver interleaving a codeword of quasi-cyclic low-density parity check codes, including repeat-accumulate quasi-cyclic low-density parity check codes,

the bit interleaver comprising:

an allocation unit allocating codeword bits of the codeword made up of N cyclic blocks each including Q bits to $Q \times N/M$ constellation words, each of the constellation words being made up of M bits, wherein

N is a multiple of M/F,

F is an integer greater than one, and is a divisor of M and Q, and

the allocation unit allocates the M bits in each of the Q/F constellation words include F bits from each of M/F different cyclic blocks in $F \times N/M$ folding sections each made up of M/F cyclic blocks.

3. A decoding method, comprising:

a demodulation step of generating a demodulated signal by demodulating a signal transmitted by modulating M bits allocated to each of a plurality of constellation words using the bit interleaving method of Claim1; and

a decoding step of decoding the demodulated signal and generating original data according to quasi-cyclic low-density parity check codes.

4. A decoder, comprising:

a demodulating unit generating a demodulated signal by demodulating a signal transmitted by modulating M bits allocated to each of a plurality of constellation words using the bit interleaver of Claim 9; and

a decoding unit decoding the demodulated signal and generating original data according to quasi-cyclic low-density parity check codes.

CLAIMS

1. A bit interleaving method for interleaving bits of a codeword generated based on a quasi-cyclic low-density parity check coding scheme, including a repeat-accumulate quasi-cyclic low-density parity check coding scheme, the bit interleaving method comprising:

a cyclic block permutation step of applying a cyclic block permutation process to a codeword made up of N cyclic blocks each consisting of Q bits, to reorder the cyclic blocks in accordance with a cyclic block permutation rule defining a reordering of the cyclic blocks;

a bit permutation step of applying a bit permutation process to the codeword after the cyclic block permutation process, to reorder the bits of the codeword in accordance with a bit permutation rule defining a reordering of the bits; and

a dividing step of dividing the codeword after the bit permutation process into a plurality of constellation words, each of the constellation words being made up of M bits, wherein

N is not a multiple of M,

the bit permutation rule defines the reordering of the bits of the codeword after the cyclic block permutation process, such that the Q bits in each of N'=N-X cyclic blocks are each allocated to a bit of an identical bit index in Q constellation words and the Q constellation words are each made up of one bit in each of M cyclic blocks, the M cyclic blocks being common to the Q constellation words, where X is a remainder of N divided by M, and

the bit index of the bit in each of the Q constellation words to which the bits in each of the N'=N-X cyclic blocks are each allocated is determined in accordance with the cyclic block permutation rule.

2. A bit interleaver for interleaving bits of a codeword generated based on a quasi-cyclic low-density parity check coding scheme, including a repeat-accumulate quasi-cyclic low-density parity check coding scheme, the bit interleaver comprising:

a cyclic block permutator applying a cyclic block permutation process to a

codeword made up of N cyclic blocks each consisting of Q bits, to reorder the cyclic blocks in accordance with a cyclic block permutation rule defining a reordering of the cyclic blocks; and

a bit permutator applying a bit permutation process to the codeword after the cyclic block permutation process, to reorder the bits of the codeword in accordance with a bit permutation rule defining a reordering of the bits; and

a divider dividing the codeword after the bit permutation process into a plurality of constellation words, each of the constellation words being made up of M bits, wherein

N is not a multiple of M,

the bit permutation rule defines the reordering of the bits of the codeword after the cyclic block permutation process, such that the Q bits in each of N'=N-X cyclic blocks are each allocated to a bit of an identical bit index in Q constellation words and the Q constellation words are each made up of one bit in each of M cyclic blocks, the M cyclic blocks being common to the Q constellation words, where X is a remainder of N divided by M, and

the bit index of the bit in each of the Q constellation words to which the bits in each of the N'=N-X cyclic blocks are each allocated is determined in accordance with the cyclic block permutation rule.

3. A signal processing method for processing a signal transmitted by modulating N×Q/M constellation words, the constellation words being generated by applying a bit reordering process to a codeword generated based on a quasi-cyclic low-density parity check coding scheme, including a repeat-accumulate quasi-cyclic low-density parity check coding scheme, and dividing bits of the codeword for each M bits, the codeword being made up of N cyclic blocks each including Q bits,

the bit reordering process comprising:

a cyclic block permutation process of reordering the cyclic blocks of the codeword in accordance with a cyclic block permutation rule defining a reordering of the cyclic blocks; and

a bit permutation process of reordering the bits of the codeword after the cyclic

block permutation process in accordance with a bit permutation rule defining a reordering of the bits, wherein

N is not a multiple of M,

the bit permutation rule defines the reordering of the bits of the codeword after the cyclic block permutation process, such that the Q bits in each of N'=N-X cyclic blocks are each allocated to a bit of an identical bit index in Q constellation words and the Q constellation words are each made up of one bit in each of M cyclic blocks, the M cyclic blocks being common to the Q constellation words, where X is a remainder of N divided by M, and

the bit index of the bit in each of the Q constellation words to which the bits in each of the N'=N-X cyclic blocks are each allocated is determined in accordance with the cyclic block permutation rule,

the signal processing method comprising:

a demodulating step of generating a demodulated signal by demodulating the signal, which has been transmitted by modulating the N×Q/M constellation words; and

a decoding step of decoding the demodulated signal in accordance with the cyclic block permutation rule and the bit permutation rule to generate data before coding according to the quasi-cyclic low-density parity check coding scheme.

4. A signal processor for processing a signal transmitted by modulating N×Q/M constellation words, the constellation words being generated by applying a bit reordering process to a codeword generated based on a quasi-cyclic low-density parity check coding scheme, including a repeat-accumulate quasi-cyclic low-density parity check coding scheme, and dividing bits of the codeword for each M bits, the codeword being made up of N cyclic blocks each including Q bits,

the bit reordering process comprising:

a cyclic block permutation process of reordering the cyclic blocks of the codeword in accordance with a cyclic block permutation rule defining a reordering of the cyclic blocks; and

a bit permutation process of reordering the bits of the codeword after the cyclic

block permutation process in accordance with a bit permutation rule defining a reordering of the bits, wherein

N is not a multiple of M,

the bit permutation rule defines the reordering of the bits of the codeword after the cyclic block permutation process, such that the Q bits in each of N'=N-X cyclic blocks are each allocated to a bit of an identical bit index in Q constellation words and the Q constellation words are each made up of one bit in each of M cyclic blocks, the M cyclic blocks being common to the Q constellation words, where X is a remainder of N divided by M, and the bit index of the bit in each of the Q constellation words to which the bits in each of the N'=N-X cyclic blocks are each allocated is determined in accordance with the cyclic block permutation rule,

the signal processor comprising:

a demodulator generating a demodulated signal by demodulating the signal, which has been transmitted by modulating the N×Q/M constellation words; and

a decoder decoding the demodulated signal in accordance with the cyclic block permutation rule and the bit permutation rule to generate data before coding according to the quasi-cyclic low-density parity check coding scheme.