

MEASURING APPARATUS

This invention relates to measuring apparatus and particularly, though not exclusively, to electronic thermometers.

A conventional electronic thermometer uses a thermosensitive element and a reference resistor. In order to adjust the accuracy of temperature measurement, a variable resistor is connected in series with the reference resistor to adjust for the deviation of the resistance ratio of the thermosensitive element and the reference resistor from a predetermined value. This conventional electronic thermometer has the following drawbacks:

1. It takes a long time to complete adjustment of the resistance ratio;
2. Absolute value adjustment is difficult to achieve with a high degree of precision;
3. Because of the cost of the variable resistor itself and the additional adjustment steps required during manufacture, the cost of the conventional electronic thermometer is relatively high.

According to one particular aspect of the present invention, there is provided a measuring apparatus comprising means for producing pulses at a rate dependent upon the value of a characteristic alternately of a first element and of a second element, means for counting the number of pulses so produced, means for controlling the operation of the pulse producing means so as to produce a predetermined number of pulses at the rate dependent upon the value of the characteristic of the first element, means to vary said

predetermined number of pulses, said varying means including means to enter additional counts into the pulse counting means prior to first element characteristic value measurement, means for measuring and storing the time taken to produce that predetermined number of pulses, means for controlling the operation of the pulse producing means to produce pulses at the rate dependent upon the value of the characteristic of the second element during the time so stored, and means for converting the number of pulses so produced during that time into a digital value to be displayed.

10 In the preferred embodiment of measuring apparatus in the form of an electronic thermometer, said first and second elements are a reference resistor and a thermosensitive element respectively.

Said pulse producing means may be a resistance-frequency converter or a double integration converter.

15 Said counter means may be a resettable $1/2$ divider circuit or a combination of a set-priority resettable $1/2$ divider for low bits and a resettable $1/2$ divider for high bits.

Said converting means may consist of a latch circuit, a read-only-memory and/or a decoder, a driver circuit and a display device.

20 The counts resulting from the first and second element measurements are proportional to the ratio of the resistances of the thermosensitive element and the reference resistor. When the count resulting from the second element measurement is to be altered in order to realise absolute value adjustment of the

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electronic thermometer, the deviation of the ratio of the resistance of the thermosensitive element to the resistance of the reference resistor is adjusted by altering the count resulting from the first element measurement. Accordingly, absolute value adjustment of an electronic thermometer is achieved by providing an initial logic adjustment circuit for detecting the count resulting from the first element measurement.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

10 Figure 1 is a block diagram of a first embodiment of an electronic thermometer according to the present invention;

 Figure 2 is a circuit diagram of a resistance-frequency

converter circuit of the electronic thermometer of Figure 1;

Figure 3 is a circuit diagram of a part of an initial logic adjustment circuit and divider network of an electronic thermometer of Figure 1;

5 Figure 4 is a timing chart illustrating the operation of the electronic thermometer of Figures 1 to 3;

Figure 5 is a circuit diagram of a modification of the initial logic adjustment circuit of Figure 3;

Figure 6 is a circuit diagram of a second embodiment of an
10 electronic thermometer according to the present invention; and

Figure 7 is a timing chart illustrating the operation of the electronic thermometer of Figure 6.

Throughout the drawings like parts have been designated by the same reference numerals.

15 Figure 1 is a block diagram of a first embodiment of an electronic thermometer according to the present invention. The principle of temperature measurement used by this electronic thermometer is as follows. First, a digital count corresponding to temperature to be measured is calculated from charging and discharging
20 operations of a reference resistor 2 and the capacitor 4 and of a thermosensitive element 3 and the capacitor 4. The digital count is then latched by a latch circuit 11 and is converted into a digital temperature value by a converting table in a read-only-memory (hereinafter referred to as "ROM") 12 to be displayed by a display portion 15.

25 In Figure 1 clock signals generated from an oscillator circuit 19 divided by a main counter 18 and fed to a main controller 17 which produces control signals $\phi 1$, $\phi 2$, $\phi 3$ at its output. The control

signals ϕ_1 , ϕ_2 , ϕ_3 are gate signals to respective MOS transistors Tr1, Tr2, Tr3 for effecting the aforementioned charging and discharging operations. The transistors Tr1, Tr2 are P-channel transistors and the transistor Tr3 is an N-channel transistor.

5 The periods of the charging and discharging operations of the reference resistor 2 and the capacitor 4 and of the thermosensitive element 3 and the capacitor 4 are defined ^{As} ~~as~~ Phase I and Phase II, respectively and these will be explained with reference to Figure 2.

In Phase I, the control signals ϕ_2 , ϕ_3 are high level (level H) and the starting level at a point B is level H and the control signal ϕ_1 is low level (level L). Since the transistors Tr1, Tr2 are P-channel transistors and the transistor Tr3 is an N-channel transistor, the transistor Tr1 turns ON. If the capacitance of the capacitor 4 is C and the resistance of the reference resistor 2 is R1, the
10 capacitor is charged with a time constant C.R1.
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An inverter 5 inverts the signal fed to its input when the level of the signal at point A exceeds the logic level of the inverter i.e. $1/2 V_{DD}$ and the inverted signal at the output of the inverter 5 is again inverted by a NAND gate 6 and applied to the gate
20 of the transistor Tr3, which immediately turns ON. Consequently, the signal at the point A is shorted to VSS through the transistor Tr3. The waveforms of the signals at points A and B in Phase I are shown in Figure 4. Given that phase I has a period T1, the relation between the period T1 and a count N1 of the pulses of the signal at
25 point B is expressed by:

$$T1 = (C \times R1 \times \ln 2) \times N1 \dots (1)$$

In Phase II, the control signal $\phi 2$ is level L and the control signals $\phi 1$, $\phi 3$ are level H and the starting level at the point B is level H and only the transistor Tr2 is ON.

Accordingly, if the resistance of the thermosensitive element

5 3 is R_s , the capacitor 4 is charged with a time constant $C.R_s$.

In the same way as described above, when the level of the signal at point A reaches the logic level of the inverter 5, i.e.

$1/2 V_{DD}$ the transistor Tr3 turns ON and the signal at the point A is shorted to VSS. The waveforms of the signals at points

10 A, B, are also shown in Figure 4.

Given that Phase II has a period T_2 , the relation between the period T_2 and the count N_2 of the pulses of the signal at point B is expressed by:

$$T_2 = (C \times R_s \times \ln 2) \times N_2 \dots\dots (2)$$

15 The period T_1 starts at the rise of a control signal $\phi 4$ from a divider stage of the main counter 18. Then, the control signal $\phi 1$ from the main controller 17 falls and the control signal $\phi 3$ rises. At this time, the charging and discharging operations of the reference resistor 2 and the capacitor 4

20 (FROM THE MAIN CONTROLLER 17 TO NOR GATE 7) commences. In response to the fall of a signal C_1 , a pulse of the signal at the point B is applied to a divider network ^{AS A} 10 ~~of the~~ clock signal. The charging and discharging operations of the reference resistor 2 and the capacitor 4 continues and when the count in the divider network 10 coincides with the

25 count N_1 of the pulses in Phase I a multiple input NAND gate 16 outputs a signal G. In response to the output of the signal G

the control signal $\phi 1$ rises and the control signal $\phi 3$ falls
and consequently, ~~the delivery of~~ the signal C ^{RISES} ~~is terminated~~,
thus terminating Phase I. At this time, the main controller
17 stores the length of the period T1 using the divided output
5 of the main counter 18. During the period T1 in Phase I, a
signal H is level H.

The period T2 starts with the fall of the control signal
 $\phi 4$. Then the control signal $\phi 2$ falls and the control signal $\phi 3$
rises when charging and discharging operations of the thermo-
10 sensitive element 3 and the capacitor 4 commences. In response
to the fall of the signal C, a pulse of the signal at point
B is applied to the divider network 10 as a clock signal. As
the charging and discharging operations of the thermosensitive
element 3 and the capacitor 4 continues, the main counter 18
15 continues to count up. At this time, by the main controller
17, a divided output DATA of a length corresponding to the
period T1 which has been stored therein in Phase I, is compared
with the counted DATA by the main counter 18. In response
to coincidence of the divided output DATA and the counted DATA,
20 the control signals $\phi 2$, $\phi 3$ from the main controller 17 rise
and fall respectively and consequently, the signal C rises,
thus terminating the period T2. At the same time, in order
to latch the count N2, the main controller 17 outputs a latch
signal ^U ~~W~~ and the count N2 is latched by the latch circuit 11.
25 As explained above, the main controller 17 operates so
as to make the length of the periods T1 and T2 equal. Accordingly,

equations (1) and (2) may be expressed as:

$$(C \times R_1 \times \ln 2) \times N_1 = (C \times R_s \times \ln 2) \times N_2 \dots (3)$$

$$N_2 = (R_1/R_s) \times N_1 \dots (4)$$

Thus, counts N_1 , N_2 are proportional to one another.

5 If a thermistor is used as the thermosensitive element, its resistance R_s at temperature T ($^{\circ}\text{C}$) is given by:

$$R_s = R_0 \text{ EXP } B (1/T - 1/T_0) \dots (5)$$

where, B is a constant of the thermistor, T_0 is a reference temperature and R_0 is the resistance of the thermistor at the
10 reference temperature T_0 .

Substituting equation (5) in equation (4) gives:

$$N_2 = R_1 / \{ R_0 \text{ EXP } B (1/T - 1/T_0) \} \times N_1 \dots (6)$$

Thus, the count N_2 over the temperature T is calculated.

The count N_2 is transmitted to the ROM 12 by the latch
15 circuit 11 and converted to a digital temperature value in
~~centigrade~~ ^{CELSIUS} ($^{\circ}\text{C}$) (or in Fahrenheit ($^{\circ}\text{F}$) by a conversion table)
based on equation (6).

The opposite case to that described above is also possible,
that is the charging and discharging operations of the thermo-
20 sensitive element 3 and the capacitor 4 is performed in Phase
I, and in Phase II, the charging and discharging operations
of the reference resistor 2 and the capacitor 4 is performed.
The charging and discharging operations of the reference resistor
and the capacitor is expressed by the count N_2 and converted
25 to a digital temperature value. This is because count N_1 , N_2
are proportional.

Absolute value adjustment will now be explained. In order to adjust the absolute value of the resistance, it is necessary to change the count N2 of the signal at point B (i.e. the count derived from the charging and discharging operations of the thermosensitive element 3 and the capacitor 4) to a predetermined count. It is necessary to correct the deviation of the count N2 because of the deviation of the resistance ratio of the reference resistor 2 and the thermosensitive element 3 from a predetermined resistance ratio due to the deviation of the reference resistor 2 and the thermosensitive element from predetermined resistance values. Given that the deviation of the real resistance ratio from the predetermined resistance ratio is K, equation (4) may be expressed as:

$$N2 = (R1/Rs) \times N1 \times K \dots (7)$$

By making the count N1 variable, which is indicated by N|| and by making N|| = N1/K, the equation (7) becomes:

$$\cancel{N2 = R1/Rs \times N|| \times K \times K} \quad N2 = (R1/Rs) \times (N||/K) \times K$$

$$N2 = (R1/Rs) \times N|| \dots (8).$$

Thus, the deviation of K from the predetermined resistance ratio is corrected when N1 = N|| and consequently the absolute value adjustment is achieved. Accordingly, in this embodiment the count N1 is varied by providing an initial logic adjustment circuit 9.

The logic adjustment circuit 9 is designed so that N|| is the difference between the output of the NAND gate 16 and predetermined initial DATA set of the initial logic adjustment

circuit 9 and $N_{||}$ is varied. Given that the output^G of the NAND gate 16 is M and the predetermined value of the initial DATA set is MO , $N_{||}$ is expressed by:

$$N_{||} = M - MO \dots (9)$$

- 5 In this embodiment, M is fixed and MO is varied so that $N_{||}$ is variable.

A method for varying MO will be described with reference to Figure 3. For example, if MO is to be 1 (i.e. $MO = 1$), a substrate pattern line between input DO of a logic adjustment
10 DATA input terminal D (hereinafter referred to as "terminal D") and a VSS line 33 is cut, so that the terminal D is pulled up by a 1/2 bit flip-flop circuit 20. The flip-flop circuit 20 outputs a DATA read-in signal J and, with response to the timing of the signal J, a NAND gate 24 turns ON to set the
15 2^0 output of a set-priority resettable 1/2 divider stage 28. Thus, MO is made to be 1.

In another example, if MO is to be 5 ($MO = 5$), not only the pattern line between the input DO of the terminal D and the VSS line 33 is cut but also the pattern line between input
20 D2 of the terminal D and the VSS line 33 is cut. Accordingly, the 2^2 output of a set 1/2 divider stage 30 as well as the 2^0 output of the resettable 1/2 divider stage 28 are set and MO becomes 5.

If any pattern line between the terminal D and the VSS
25 line 33 is not cut, the output of the corresponding 1/2 resettable divider stage is not set.

Additionally, when P-channel transistors Tr4 to Tr7 are ON all the time, current always flows between VDD and VSS and so the power consumption of the circuit increases. Accordingly, since initial DATA is required to be read in an appropriate

5 cycle so that the transistors Tr4 to Tr7 turn ON in response to a signal of level L to a gate terminal 34 and the DATA read-in signal is fed to a clock terminal 35 to provide initial DATA to the 1/2 bit flip-flop circuits 20 to 23 and the initial DATA is held until the following data read-in cycle. In Figure

10 3, reference numbers 24,25,26,27 indicate NAND gates, reference numerals 28,^{29,30}31 indicate set 1/2 dividers and reference numeral 32 indicates a resettable 1/2 divider stage.

As shown by Figure 4, the timing of providing the initial DATA is such that after all dividers in the divider network

15 10 are reset by a reset signal I before the beginning of Phase I, logic adjustment DATA, i.e. the initial DATA is read-in in response to the signal J.

As mentioned above, in this embodiment, the predetermined value of the initial DATA set is defined by inputting the logic

20 adjustment DATA by selectively cutting substrate pattern lines to inputs D0 to D3 ^{to} (OF THE FLIP-FLOP CIRCUITS 20 TO 23) ~~of~~ the terminals D. Accordingly, the count N1 of the charging and discharging operations of the reference resistor 2 and the capacitor 4 during the period T1 in Phase I can be varied and thus the deviation of the resistance ratio

25 due to the deviation of the resistance of the thermosensitive

element and the reference resistor can be corrected, consequently achieving absolute value adjustment.

Figure 5 shows a modification of the initial logic adjustment circuit of Figure 3. First, the reference resistance is converted to a corresponding frequency a predetermined number of times (the number of times being determined by the output of a multi-input NAND gate 129 in the initial logic adjustment circuit). Then the resistance of the thermosensitive element is converted to a corresponding frequency for a time which is defined by the main counter 18 and the main controller 17 and which is equal to the time for the reference resistance-frequency conversion. The resulting count of the resistance-frequency conversion with respect to the resistance of the thermosensitive element is latched by the latch circuit 11, whose output is, in turn, decoded by the decoder 13 to be displayed by the display ^{PORTION} device 15.

Since the resistance-frequency conversions with respect to the resistance of the reference resistor and the resistance of the thermosensitive element are performed in a fixed period of time and with respect to the resistance-frequency conversion, the resistance is in inverse proportion to the number of conversions, the conversion of the resistance to the count over temperature of the thermosensitive element is expressed by the following equation:

$$R_l \times L = R_s \times N \dots (10)$$

where, L is the predetermined count of the reference resistance-

frequency conversion, ~~i is the predetermined count of the~~
~~reference resistance-frequency conversions~~, N is the predetermined
count of the resistance-frequency conversion with respect to
the resistance of the thermosensitive element, R₁ is the resistance
5 of the reference resistor and R_s is the resistance of the thermo-
sensitive element.

In initial adjustment, the predetermined count N of the
resistance-frequency conversion with respect to the resistance
of the thermosensitive element is adjusted. So, by transforming
10 equation (10), N is obtained as follows:

$$N = L \times (R_1/R_s) \dots\dots (11)$$

Accordingly, the deviation of the ratio (R₁/R_s) is corrected
by L. Given that in this embodiment the count of the output
of the multi-input NAND gate 129 is W, W corresponds to L.

15 The value W can be varied according to the states of the initial
logic adjustment DATA input lines (hereinafter referred to
as "DATA line") D₀, D₁, D₂, D₃ which are applied to one input
of exclusive OR gates (EXOR) 124, 125, 126, 127, respectively.
Consequently, the value L of equation (11) is varied, thus
20 enabling logic adjustment.

To be more comprehensive, the above principle will be
explained using actual figures. If the resistance of the thermo-
sensitive element and the resistance of the reference resistance
over temperature at the time of adjustment are 23.0kΩ and 22.4kΩ,
25 respectively, the count N of the resistance-frequency conversions
with respect to the resistance of the thermosensitive element

is adjusted to 224 counts, L is obtained by substitution in equation (11):

$$224 = L \times 22.4/23.0 \dots (12)$$

consequently $L = 230$.

- 5 Accordingly, in this example, the initial adjustment is realised by setting W to 230 counts.

If the output of each resettable 1/2 divider stage 115 to 122 is VDD and the division ratio of each can be predetermined (for example 2^0 for the presettable 1/2 divider stage and 2^1 for the resettable divider stages) W is calculated as below:

$$\begin{aligned} W &= 230 \\ &= 128 + 64 + 32 + 4 + 2 \\ &= 2^7 + 2^6 + 2^5 + 2^2 + 2^1 \end{aligned}$$

So, in order to predetermine W at 218, the multi-input NAND gate is designed to produce an output when outputs of 2^7 , 2^6 , 2^5 , 2^2 , 2^1 of the resettable 1/2 divider stages are VDD and the outputs of 2^4 , 2^3 , 2^0 of the remaining resettable 1/2 divider stages are VSS.

In order to design the multi-input NAND gate 129 to produce the desired output, the following is necessary:

- (1) The multi-input NAND gate 129 outputs VSS when all inputs thereto are VDD.
- (2) When inputs from inputs D0 to D3 to the EXORs are VDD, the outputs of the respective resettable 1/2 divider stages of the divider network 10 are inverted by the EXORs and the inverted outputs are fed to the multi-input NAND gate 129.

(3) When the inputs from inputs D0 to D3 to the EXORs are VSS, the outputs of the respective resettable 1/2 divider stages pass through the EXORs and are fed to the multi-input NAND gate 129.

5 Considering the above points, in the above actual example circuitry is arranged so that the EXORs 125, 126 pass the outputs of the respective resettable 1/2 divider stages to the multi-input NAND gate without inversion and the EXORs 124, 127 invert the outputs of the respective resettable 1/2 divider
10 stages applied thereto and apply the inverted outputs to the multi-input NAND gate. Accordingly, by determining inputs D1, D2 to be VSS and inputs D0, D3 to be VDD, W becomes 230.

By properly determining the number of resettable 1/2 divider stages, the number of inputs D0 to D3 and the number of outputs
15 of the multi-input NAND gate, precise adjustment is achieved with any thermosensitive element with any characteristic.

Referring again to Figure 1, if the ~~latch~~ signal E of the NAND gate 8, that is the signal ^B~~E~~ in Figure 4, is detected by an external measuring device (not shown) whose measuring
20 time is synchronised with the signal ^C~~E~~, the count N2 in relation to the measured temperature can be detected. If the count N2 is detected, the deviation of the resistance ratio of the thermosensitive element and the reference resistor before adjustment can be detected by conversion of the count N2.

25 Furthermore, if an external CPU for storing the amount of correction of the deviation of the resistance ratio for the

conversion of the count N2, that is logic adjustment DATA is provided and if the logic adjustment DATA set is performed by the external CPU using the count N2 detected as above, the logic adjustment can be completed in one step.

5 Moreover, the easy precision test of the temperature measurement of an electronic thermometer can be realised by using the ~~latch~~ signal E.

Figure 6 is a block diagram of a second embodiment of an electronic thermometer according to the present invention
10 and Figure 7 is a timing chart of the signals appearing in the electronic thermometer of Figure 6 showing the levels at specified points. In the first embodiment of the present invention, a resistance-frequency converter circuit is used, while in this embodiment a double integrating analog-digital (hereinafter
15 referred to as "AD") converter is used.

The principle of the temperature measurement of the second embodiment is that the ratio of the time required for integrating the constant voltage of the thermosensitive element 3 and a capacitor 50 and of the reference resistor 2 and the capacitor 50
20 is converted to a digital value and the temperature is displayed digitally.

The period for integration by the reference resistor 2 and the capacitor 50 and that by the thermosensitive element 3 and the capacitor 50 are referred to as a first integration
25 and a second integration, respectively, each of which is explained below.

In response to a clock signal Y1 from the oscillator circuit 65, a divider network 57 counts up from a count of 0. When the output from the divider network 57 equals the predetermined input to a multi-input NAND gate 64, the latter
5 outputs a signal Y4, which is fed to a main controller 66. Then the main controller 66 outputs a high level signal Q1 to an analog switch 54 which turns ON. The first integration is commenced at this time and terminates with the count-up of the divider circuit 57.

10 In the first integration as above, the fluctuation of the voltage of an output signal P1 of an operational amplifier OP1 is expressed by:

$$\Delta VP1 = (E2/R1) \times N1 \dots (13)$$

in which $\Delta VP1$ is the fluctuation of the voltage of the output
15 signal P1, E2 is the voltage applied to the reference resistor 2 from a reference voltage e2 and N1 is the count of the clock signals applied to the divider network 57 by the oscillator circuit 65 during the first integration.

When the first integration is complete, outputs Q1, Q2
20 of the main controller 66 become level L and level H, respectively, and accordingly analog switch 53 turns ON. The second integration then commences. As the integration continues and when the voltage level of the output of the operational amplifier OP1 reaches the level before the first integration is commenced, an operational
25 amplifier OP2 inverts the input signal thereto. This inverted signal P2 is fed to the main controller 66 which outputs a signal

Q2 of level L for terminating the second integration.

The fluctuation of the voltage of the input signal P1 of the operational amplifier OP1 during the period of the second integration is expressed by:

5
$$\Delta VP1 = (E1/Rs) \times N2 \dots (14)$$

in which E1 is the voltage applied to the thermosensitive element 3 from a reference voltage e1 and N2 is the count of clock signals counted by the divider network 57 during the second integration.

10 Since the absolute value of VP1 in equations (13) and (14) are equal, the following is obtained:

$$(E2/R1) \times N1 = (E1/Rs) \times N2 \dots (15)$$

If the circuit is designed so that the voltages E1, E2 are equal, then:

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$$N1/R1 = N2/Rs \dots (16)$$

Accordingly,

$$N2 = (Rs/R1) \times N1 \dots (17).$$

Equation (17) is the same as equation (4) above except it contains the reciprocal of R1/Rs. Consequently, similar to the first
20 embodiment, in the second embodiment deviation of the resistance ratio of the resistance of the thermosensitive element and the resistance of the reference resistor can be corrected by selecting the value of the count N1 and absolute value adjustment is achieved.

25 In the second embodiment, the phase of the output signal from the divider network is varied according to the logic

adjustment DATA and the predetermined value of the output of the multi-input NAND gate is varied using the initial logic adjustment described in relation to Figure 5. The count N1 is given by:

5
$$N1 = NO - NG \dots (18)$$

in which NO is the count of the count 0 to the count-up by the divider network 57 and NG is the predetermined value of the output of the multi-input NAND gate 64. Accordingly, by varying NG, the count N1 can be determined.

10 Figure 6 also shows an initial logic adjustment circuit 63, a resistor 49 for automatically returning to zero and analog switches 55, 56.

The present invention is applicable to any electronic thermometer, no matter what kind of AD converter is used,
15 as long as the electronic thermometer uses a system in which the resistance ratio of the thermosensitive element and the reference resistor is converted to a digital temperature value.

By properly arranging the number of bits of the logic adjustment DATA, the number of resettable 1/2 divider stages
20 and the output of the multi-input gate, deviation of resistance of any thermosensitive element and reference resistor can be corrected and, since the adjustment is done in one clock period, adjustment to a high degree of precision is achievable.

Moreover, in accordance with the present invention, the
25 divider network or the main counter is used as a round counter for counting in a round cycle from count 0 to a count-up value.

Since a round counter provides a constant measurement cycle regardless of the result of measurement, an external CPU can be easily connected. Also, by further dividing the round cycle, the time for generating a buzzer sound or for automatically
5 disconnecting a power supply can be set. Thus, the number of resettable $1/2$ divider stages required for obtaining the round cycle is reduced. As a matter of course, it is also possible that a specially constructed divider network can be used instead of a round counter.

10 Still further, it is also within the scope of the present invention if the main counter, the main controller, the initial logic adjustment circuit, divider circuits, the multi-input gates, the latch circuits, ROM, the decoder, the driver circuit, etc. are replaced by an appropriate one-chip or two-chip CPU
15 as required. When a CPU is used, a fuse ROM or a programmable ROM can be used for holding logic adjustment DATA.

In the above description of the preferred embodiment of the present invention, deviation of the resistance ratio of a thermosensitive element and a reference resistor is corrected
20 by variously determining the count of a first clock to realise absolute value adjustment.

By similarly arranging the number of bits of logic adjustment DATA, any deviation of the resistance ratio can be adjusted. Also, adjustment is performed in respect of one clock of the
25 count and adjustment to a high degree of precision can be achieved.

As to cost of an electronic thermometer according to the present invention, a variable resistor required by conventional electronic thermometers is not necessary, so that the time required for adjustment is reduced, etc. and together these
5 lead to a reduction in cost compared to conventional electronic thermometers. Since a variable resistor is not necessary, an electronic thermometer according to the present invention is shock-resistant and has improved aging characteristics. Moreover, the absence of a variable resistor enables size to
10 be reduced.

The present invention is applicable not only to electronic thermometers such as clinical thermometers, but also to manometers and other measuring devices.



CLAIMS

1. A measuring apparatus comprising means for producing pulses at a rate dependent upon the value of a characteristic alternately of a first element and of a second element, means for counting the number of pulses so produced, means for controlling the operation
5 of the pulse producing means so as to produce a predetermined number of pulses at the rate dependent upon the value of the characteristic of the first element, means to vary said predetermined number of pulses, said varying means including means to enter additional counts into the pulse counting means prior to first
10 element characteristic value measurement, means for measuring and storing the time taken to produce that predetermined number of pulses, means for controlling the operation of the pulse producing means to produce pulses at the rate dependent upon the value of the characteristic of the second element during the time so
15 stored, and means for converting the number of pulses so produced during that time into a digital value to be displayed.
2. Apparatus as claimed in claim 1, in which said first and second elements are a reference resistor and a thermosensitive element, respectively.
- 20 3. Apparatus as claimed in claim 1 or 2, in which said pulse producing means is a resistance-frequency converter or a double integration converter.
4. Apparatus as claimed in any preceding claim, in which said pulse counting means is a resettable $1/2$ divider circuit or a
25 combination of a set-priority resettable $1/2$ divider for low bits and a resettable $1/2$ divider for high bits.



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5. Apparatus as claimed in any preceding claim, in which said converting means consists of a latch circuit, a read-only-memory and/or a decoder, a driver circuit and a display device.
6. An electronic thermometer substantially as herein described
- 5 with reference to and as shown in Figures 1 to 4 of the accompanying drawings.
7. An electronic thermometer substantially as herein described with reference to Figures 1 to 4 and as modified in Figure 5 of the accompanying drawings.
- 10 8. An electronic thermometer substantially as herein described with reference to Figures 6 and 7 of the accompanying drawings.