C L A I M S

1. A semiconductor memory device, comprising a first chip including:

a first substrate that includes a first via and a second via; and

a first element layer provided on an upper surface of the first substrate, and that includes a first pad and a second pad on an upper surface of the first element layer; and

a second chip including:

a second substrate that includes a third via and a fourth via; and

a second element layer provided on an upper surface of the second substrate, and that includes a third pad and a fourth pad on an upper surface of the second element layer, wherein

the upper surface of the second element layer is arranged so as to be opposed to the upper surface of the first element layer,

the first and third pads, and the second and fourth pads are symmetrically arranged with respect to a surface where the first element layer and the second element layer are opposed to each other, and the first and third pads, and the second and fourth pads are electrically coupled,

the first element layer and the second element layer further include:

a first signal line that electrically couples the first via to the third via through the first pad and the third pad;

at least one logic circuit that is provided on a path of the first signal line; and

a second signal line that electrically couples the second via to the fourth via through the second pad and the fourth pad without involving the at least one logic circuit,

the first element layer includes a first logic circuit that is provided on a path of the first signal line, and includes an input terminal electrically coupled to the first via and an output terminal electrically coupled to the first pad, and

the second element layer includes a second logic circuit that is provided on a path of the first signal line, and includes an input terminal electrically coupled to the output terminal of the first logic circuit through the first pad and the second pad, and an output terminal electrically coupled to the second via.

2. The semiconductor memory device according to claim 1, wherein

the first and second logic circuits are symmetrically arranged with respect to the surface where the first element layer and the second element layer are opposed to each other.

3. The semiconductor memory device according to claim 1, wherein

the first and second logic circuits are asymmetrically arranged with respect to the surface where the first element layer and the second element layer are opposed to each other.

4. The semiconductor memory device according to claim 3, wherein

the first element layer and the second element layer are provided in accordance with a same layout pattern.

5. The semiconductor memory device according to claim 3, wherein

the first element layer and the second element layer are provided in accordance with different layout patterns.

6. The semiconductor memory device according to claim 1, wherein

each of the first element layer and the second element layer are included in different core chips, respectively.

7. The semiconductor memory device according to claim 1, wherein

the first element layer and the second element layer are included in a same core chip.

8. The semiconductor memory device according to claim 1, further comprising a third chip including:

a third substrate that includes a fifth via and a sixth via; and

a third element layer provided on an upper surface of the third substrate, and that includes a fifth pad and a sixth pad on an upper surface of the third element layer, wherein

a lower surface of the third substrate is arranged so as to be opposed to a lower surface of the second substrate,

the third and fifth vias, and the fourth and sixth vias are symmetrically arranged with respect to a surface where the second substrate and the third substrate are opposed to each other, and the third and fifth vias, and the fourth and sixth vias are electrically coupled, and

the first signal line electrically couples the first via to the fifth pad further through the third via and the fifth via, and the second signal line electrically couples the second via to the sixth pad further through the fourth via and the sixth via without involving the at least one logic circuit.

9. The semiconductor memory device according to claim 8, wherein

the third and fifth pads, and the fourth and sixth

pads are symmetrically arranged with respect to the surface where the second substrate and the third substrate are opposed to each other.

10. The semiconductor memory device according to claim 9, further comprising a fourth chip including:

a fourth substrate that includes a seventh via and a eighth via; and

a fourth element layer provided on an upper surface of the fourth substrate, and that includes a seventh pad and an eighth pad on an upper surface of the fourth element layer, wherein

the upper surface of the fourth element layer is arranged so as to be opposed to the upper surface of the third element layer,

the fifth and seventh pads, and the sixth and eighth pads are symmetrically arranged with respect to a surface where the third element layer and the fourth element layer are opposed to each other, and the fifth and seventh pads, and the sixth and eighth pads are electrically coupled,

the first signal line electrically couples the first via to the seventh via further through the fifth pad and the seventh pad,

the second signal line electrically couples the second via to the eighth via further through the sixth pad and the eighth pad without involving the at least one logic circuit.

11. The semiconductor memory device according to claim 10, wherein

the first and seventh pads, and the second and eighth pads are symmetrically arranged with respect to the surface where the second substrate and the third substrate are opposed to each other.

12. The semiconductor memory device according to claim 11, wherein

the first and third vias, and the second and fourth vias are symmetrically arranged with respect to the surface where the first element layer and the second element layer are opposed to each other.

13. The semiconductor memory device according to claim 11, wherein

the first and third vias, and the second and fourth vias are asymmetrically arranged with respect to the surface where the first element layer and the second element layer are opposed to each other.

14. The semiconductor memory device according to claim 10, wherein

the first element layer, the second element layer, and the third element layer are included in a same core chip.

15. The semiconductor memory device according to claim 10, wherein

the first element layer and the third element layer are provided in accordance with a same layout pattern.

16. The semiconductor memory device according to claim 8, wherein

the first element layer and the third element layer are provided in accordance with different layout patterns.

17. The semiconductor memory device according to claim 1, wherein

the first substrate further includes a ninth via and a tenth via,

the first element layer further includes a ninth pad arranged at a position symmetric to the first pad, and a tenth pad arranged at a position symmetric to the second pad, with respect to a center of the first element layer in the upper surface of the first element layer,

the second substrate further includes an eleventh via and a twelfth via,

the second element layer further includes an eleventh pad arranged at a position symmetric to the third pad, and a twelfth pad arranged at a position symmetric to the fourth pad, with respect to a center of the second element layer in the upper surface of the second element layer,

the ninth and eleventh pads, and the tenth and twelfth

pads are symmetrically arranged with respect to the surface where the first element layer and the second element layer are opposed to each other, and the ninth and eleventh pads, and the tenth and twelfth pads are electrically coupled,

the first element layer and the second element layer further include:

a third signal line that electrically couples the ninth via to the eleventh via through the ninth pad and the eleventh pad,

at least one logic circuit that is provided on a path of the third signal line, and

a fourth signal line that electrically couples the tenth via to the twelfth via through the tenth pad and the twelfth pad without involving the at least one logic circuit provided on the path of the third signal line.

18. The semiconductor memory device according to claim 17, wherein

the first via, the second via, the third via, the fourth via, the first pad, the second pad, the third pad, and the fourth pad are included in a first core chip,

the ninth via, the tenth via, the eleventh via, the twelfth via, the ninth pad, the tenth pad, the eleventh pad, and the twelfth pad are included in a second core chip.

19. The semiconductor memory device according to

claim 4 or 5, wherein

the first element layer further includes a first peripheral circuit electrically coupled to the first signal line, and

the second element layer further includes a second peripheral circuit that corresponds to the first peripheral circuit and is electrically cut off from the second signal line.

20. The semiconductor memory device according to claim 7, wherein

the first element layer further includes a first portion of a peripheral circuit electrically coupled to the first signal line,

the second element layer further includes a second portion of the peripheral circuit electrically coupled to the second signal line, and

the first portion of the peripheral circuit and the second portion of the peripheral circuit include a regions overlapping in a stacking direction.

21. The semiconductor memory device according to claim 17, wherein

the first element layer further includes a shared circuit, and

the shared circuit is shared between a first portion of the first element layer and a second portion of the

first element layer.

22. A manufacturing method for a semiconductor memory device comprising:

forming a first element layer on an upper surface of a first wafer, and a second element layer on an upper surface of a second wafer;

bonding the first wafer to the second wafer with an upper surface of the first element layer being opposed to an upper surface of the second element layer;

probing a lower surface of the first wafer and a lower surface of the second wafer that are bonded to each other; and

generating two or more chip sets by simultaneously dicing the probed first and second wafers,

wherein forming the first element layer and the second element layer includes:

forming a first pad and a second pad on the upper surface of the first element layer;

forming, on the upper surface of the second element layer, a third pad at a position symmetric to the first pad and a fourth pad at a position symmetric to the second pad with respect to a surface where the first element layer and the second element layer are opposed to each other;

forming a first portion of a first signal line electrically coupled to the first pad, a first portion of a second signal line electrically coupled to the second pad,

a second portion of the first signal line electrically coupled to the third pad, and a second portion of the second signal line electrically coupled to the fourth pad; and

forming at least one logic circuit on a path of the first signal line.

23. The manufacturing method for the semiconductor memory device according to claim 22, wherein

the first element layer and the second element layer are provided in accordance with a same mask set.

24. The manufacturing method for the semiconductor memory device according to claim 23, wherein

in one of the two or more chip sets, the first and second element layers are provided in accordance with different layout patterns.

25. The manufacturing method for the semiconductor memory device according to claim 24, wherein

in one of the two or more chip sets, the first and second element layers are symmetrically arranged with respect to the surface where the first element layer and the second element layer are opposed to each other.

26. The manufacturing method for the semiconductor memory device according to claim 25, wherein

in one of the two or more chip sets, the first and second element layers are provided in accordance with different interconnect patterns.

27. The manufacturing method for the semiconductor memory device according to claim 23, wherein

in one of the two or more chip sets, the first and second element layers are provided in accordance with a same layout pattern.

28. The manufacturing method for the semiconductor memory device according to claim 22, wherein

in one of the two or more chip sets, an arrangement pattern of terminals used for probing of the lower surface of the first wafer is different from an arrangement pattern of terminals used for probing of the lower surface of the second wafer.

29. The manufacturing method for the semiconductor memory device according to claim 22, wherein

in one of the two or more chip sets, an arrangement pattern of terminals used for probing of the lower surface of the first wafer is the same as an arrangement pattern of terminals used for probing of the lower surface of the second wafer.

30. The manufacturing method for the semiconductor

memory device according to claim 22, wherein

in one of the two or more chip sets, the first and second element layers are included in different core chips.

31. The manufacturing method for the semiconductor memory device according to claim 22, wherein

in one of the two or more chip sets, the first and second element layers are included in a same core chip.

32. The manufacturing method for the semiconductor memory device according to claim 22, wherein

in one of the two or more chip sets,

the first element layer includes a first portion of a first core chip, and a first portion of a second core chip, and

the second element layer includes a second portion of the first core chip and a second portion of the second core chip.