

Abstract

A voltage applied to a bit line (BL1) or a voltage applied to a source line (SL) is reduced to a value that allows a first select gate structure (5) or a second select gate structure (6) to block electrical connection between the bit line (BL1) and a channel layer (CH) or between the source line (SL) and the channel layer (CH), irrespective of a charge storage gate voltage needed to inject charge into a charge storage layer (EC) by a quantum tunneling effect. In accordance with the reduction in voltage(s) applied to the bit line (BL1) and the source line (SL), thickness of a first select gate insulating film (30) of the first select gate structure (5) and thickness of a second select gate insulating film (33) of the second select gate structure (6) are reduced. High-speed operation is achieved correspondingly. In accordance with the reduction in voltage(s) applied to the bit line (BL1) and the source line (SL), thickness of a gate insulating film of a field effect transistor in a peripheral circuit that controls a memory cell is reduced. The area of the peripheral circuit is reduced correspondingly.