ZERO-CROSSING COMPARATORS WITH THRESHOLD VALIDATION

Voltage comparators and other circuits for slicing analogue signals are well known in the art and employed in many situations. In some applications where the need exists to distinguish a valid signal from low level noise, a voltage threshold may be applied to the reference input of the comparator in order that only signals exceeding that threshold voltage will cause the comparator to switch. Unfortunately when this method is used, the transition of the comparator output will be delayed with reference to the zero-crossing of the input in one direction and advanced in the other direction by an amount depending upon the amplitude of the input signal. In some applications like carrier recovery and timing recovery systems in high performance data modems it is essential to preserve accurately the zero-crossing instant of the input while providing a threshold to prevent the comparator responding to signals of less than a predetermined amplitude. It is an aim of the present invention to achieve this preservation.

According to the invention there is provided a circuit arrangement for use in carrier and timing recovery circuits of a digital data transmission system, the arrangement being adapted to generate an output signal (OPS) when an input signal (IPS) crosses zero on condition that the excursion of the input signal has exceeded a reference threshold signal (+VE) during the

previous half cycle, including first (C1) and second (C2) differential amplifiers both of which are connected to receive the input signal (IPS) and further including a toggle (D1) characterised in that the first differential amplifier (C1) is arranged to produce an output signal when the input signal passes through zero in a first direction, the second differential amplifier (C2) being arranged to produce an output signal when the input signal falls in the said first direction below a predetermined threshold value, the output signal of the first differential amplifier (C1) is fed to the toggle (D1) and the output signal of the second differential amplifier (C2) being fed to a second toggle (D2), the first (D1) and second (D2) toggles are interconnected in such a manner that the first toggle (D1) produces a short pulse in response to the zero transition of the input signal when the input signal has exceeded the reference threshold in the previous half cycle.

In order that the invention may be more readily understood reference is made to the following figures.

Figure 1 illustrates the operation of a simple comparator (prior art).

Figure 2 illustrates the operation of a comparator with a threshold voltage (prior art).

Figure 3 illustrates the principle of amplitude validation of zero-crossing transitions.

Figure 4 illustrates an embodiment of the present invention comprising two comparators and bistable

storage elements which produces a narrow pulse in response to the negative zero-crossing transition of the input signal provided that the input signal has exceeded the positive reference threshold applied to the second comparator.

In Fig. 1 (prior art) the input signal IPS is applied to the positive input of a differential amplifier comparator COMP which is biased on its negative input by a zero volt OV condition. The waveforms shown at the side of the circuit of Fig. 1 indicate the input signal voltage IPSV and the output signal voltage OPSV as a function of time t. Each time the input signal crosses zero the comparator produces an output until the signal returns to zero again.

In Fig. 2 (prior art) the same comparator COMP is provided with a variable threshold level VT which provides a pedestal above zero for the comparator. The waveforms relevant to the circuit of Fig. 2 are shown at the side of the circuit and it will be seen that the threshold voltage causes displacement of A1 and A2 to be experienced from the zero crossing instants ZCI1 and ZCI2.

Fig. 3 illustrates the principle of operation of the invention in that the zero transition of the input signal IPSV is amplitude validated.

Considering now Fig. 4 an embodiment of the invention is shown in that two differential amplifier comparators C1 and C2 are provided driving a pair of

"D" type toggles D1 and D2 which are interconnected so as to generate a narrow pulse on the output lead OPS when the input lead IPS passes through zero after having exceeded the positive threshold provided by the threshold level + VT. The output signals from the comparators C1 and C2 are connected respectively to the clock inputs of the "D" type toggles while the data inputs to the "D" type toggles are held at the logic "1" state level. The Q output from toggle D2 is used to control the clear input to toggle D1 while the $\overline{Q}$ output from toggle D1 is used to control the clear input to toggle D2. In operation when the positive half cycle of the input signal falls below the threshold level +VT toggle D2 is set by the output from causing comparator C2. This causes toggle D1 to be primed on its clear input by the "1" state signal on Q2. When the input waveform IPS reaches zero comparator C1 generates an output condition to switch D1 to the "1" state. The "0" transition on $\overline{Q1}$ causes toggle D2 to be cleared which in turn switches Q2 to the "0" state thereby clearing D1. The output signal OPS, therefore, exists for the time it takes to clear toggles D2 and D1.

The above description has concentrated on circuit arrangements operating on positive signals, whereas it will be obvious to those skilled in the art how the circuits could be amended to operate on negative half cycles.

CLAIMS:-

1. A circuit arrangement for use in carrier and timing recovery circuits of a digital data transmission system, the arrangement being adapted to generate an output signal (OPS) when an input signal (IPS) crosses zero on condition that the excursion of the input signal has exceeded a reference threshold signal (+VE) during the previous half cycle, including first (C1) and second (C2) differential amplifiers both of which are connected to receive the input signal (IPS) and further including a toggle (D1) characterised in that the first differential amplifier (C1) is arranged to produce an output signal when the input signal passes through zero in a first direction, the second differential amplifier (C2) being arranged to produce an output signal when the input signal falls in the said first direction below a predetermined threshold value, the output signal of the first differential amplifier (C1) is fed to the toggle (D1) and the output signal of the second differential amplifier (C2) being fed to a second toggle (D2), the first (D1) and second (D2) toggles are interconnected in such a manner that the first toggle (D1) produces a short pulse in response to the zero transition of the input signal when the input signal has exceeded the reference threshold in the previous half cycle.

2. A circuit arrangement according to claim 1, in which the first (D1) and second (D2) toggles are D type toggles and the outputs of the differential amplifiers

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(C1 and C2) are connected respectively to the clock input (CLK) of the toggles (D1 and D2).

3. A circuit arrangement substantially as herein described with reference to Fig. 4 of the accompanying drawings.

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