

What is claimed is:

1. A three-dimensional semiconductor memory device, comprising:

an electrode structure comprising a plurality of gate electrodes and a plurality of insulating layers, wherein the gate electrodes and the insulating layers are alternately stacked on a substrate;

a semiconductor pattern extending in a first direction substantially perpendicular to a top surface of the substrate and penetrating the electrode structure;

a tunnel insulating layer disposed between the semiconductor pattern and the electrode structure;

a blocking insulating layer disposed between the tunnel insulating layer and the electrode structure; and

a charge storing layer disposed between the blocking insulating layer and the tunnel insulating layer,

wherein the charge storing layer comprises:

a plurality of first charge trap layers having a first energy band gap; and

a second charge trap layer having a second energy band gap larger than the first energy band gap,

wherein the first charge trap layers are embedded in the second charge trap layer between the gate electrodes and the semiconductor pattern, and

wherein the second charge trap layer includes a first portion disposed between the tunnel insulating layer and the first charge trap layers, a second portion disposed between the blocking insulating layer and the first charge trap layers, and the first and second portions have a same energy bandgap.

2. The three-dimensional semiconductor memory device of claim 1, wherein side surfaces of the insulating layers are spaced apart from a side surface of the semiconductor pattern by a first distance in a second direction substantially parallel to the top surface of the substrate, and

5 side surfaces of the gate electrodes are spaced apart from the side surface of the semiconductor pattern by a second distance in the second direction, wherein the second distance is larger than the first distance.

3. The three-dimensional semiconductor memory device of claim 2, wherein the charge storing layer has a first thickness between the gate electrodes and the semiconductor pattern in the second direction, and has a second thickness between the insulating layers and the semiconductor pattern in the second direction, wherein the second thickness is smaller than the first thickness.

15 4. The three-dimensional semiconductor memory device of claim 2 or claim 3, wherein each of the first charge trap layers is thicker than the second charge trap layer in the second direction.

20 5. The three-dimensional semiconductor memory device of any one of claims 1 to 4, wherein each of the first charge trap layers surrounds a portion of the semiconductor pattern.

6. The three-dimensional semiconductor memory device of any one of claims 1 to 5, wherein the second energy band gap of the second charge trap layer is smaller than a third

energy band gap of the tunnel insulating layer.

7. The three-dimensional semiconductor memory device of any one of claims 1 to 6, wherein the first charge trap layers have a first conduction band energy level,

5 the second charge trap layer has a second conduction band energy level, and

the tunnel insulating layer has a third conduction band energy level,

wherein a difference between the first and second conduction band energy levels is greater than a difference between the second and third conduction band energy levels.

10 8. The three-dimensional semiconductor memory device of any one of claims 1 to 7, wherein the second charge trap layer covers top and bottom surfaces of the first charge trap layers.

15 9. The three-dimensional semiconductor memory device of any one of claims 1 to 8, wherein the second charge trap layer is disposed between the gate electrodes and the semiconductor pattern, and the second charge trap layer is disposed between the insulating layers and the semiconductor pattern.

20 10. The three-dimensional semiconductor memory device of any one of claims 1 to 9, wherein the blocking insulating layer and the tunnel insulating layer extend in the first direction, and the blocking insulating layer contacts the tunnel insulating layer in an area between the insulating layers and the semiconductor pattern.

11. The three-dimensional semiconductor memory device of any one of claims 1

to 10, wherein the first charge trap layers comprise polysilicon, germanium (Ge), tungsten (W), nickel (Ni), or platinum (Pt), and the second charge trap layer comprises silicon nitride or silicon oxynitride.

5 12. A three-dimensional semiconductor memory device, comprising:

an electrode structure comprising a plurality of gate electrodes and a plurality of insulating layers,

wherein the gate electrodes and the insulating layers are alternately stacked on a substrate, and a side surface of the electrode structure is recessed in areas corresponding to the gate electrodes to define a plurality of recess regions;

10 a semiconductor pattern extending in a first direction substantially perpendicular to a top surface of the substrate and crossing the side surface of the electrode structure;

a plurality of first charge trap layers respectively disposed in the recess regions of the electrode structure, wherein the first charge trap layers surround the semiconductor pattern;

15 a tunnel insulating layer disposed between the first charge trap layers and the semiconductor pattern;

a blocking insulating layer disposed between the first charge trap layers and the electrode structure; and

a second charge trap layer,

20 wherein the second charge trap layer continuously extends between the blocking insulating layer and the first charge trap layers, and the second charge trap layer continuously extends between the tunnel insulating layer and the first charge trap layers,

wherein the first charge trap layers are formed of a material having a first energy band gap, and the second charge trap layer is formed of a material having a second energy band gap

larger than the first energy band gap, and

wherein the second charge trap layer includes a first portion disposed between the tunnel insulating layer and the first charge trap layers, a second portion disposed between the blocking insulating layer and the first charge trap layers, and the first and second portions have a same energy bandgap.

13. The three-dimensional semiconductor memory device of claim 12, wherein the second charge trap layer contacts top and bottom surfaces of each of the first charge trap layers.

14. The three-dimensional semiconductor memory device of claim 12 or claim 13, wherein the second charge trap layer extends in the first direction.

15. The three-dimensional semiconductor memory device of any one of claims 12 to 14, wherein the blocking insulating layer contacts the tunnel insulating layer in an area between the insulating layers and the semiconductor pattern.

16. The three-dimensional semiconductor memory device of any one of claims 12 to 15, wherein the blocking insulating layer extends in the first direction, and conformally covers the recess regions of the electrode structure.

17. The three-dimensional semiconductor memory device of any one of claims 12 to 16, wherein the second energy band gap of the second charge trap layer is smaller than a third energy band gap of the tunnel insulating layer.

18. The three-dimensional semiconductor memory device of any one of claims 12 to 17, wherein the first charge trap layers have a first conduction band energy level,
the second charge trap layer has a second conduction band energy level, and
5 the tunnel insulating layer has a third conduction band energy level,
wherein a difference between the first and second conduction band energy levels is greater than a difference between the second and third conduction band energy levels.

19. The three-dimensional semiconductor memory device of any one of claims 12 to 18, wherein the tunnel insulating layer extends in the first direction and surrounds a side
10 surface of the semiconductor pattern.

20. The three-dimensional semiconductor memory device of any one of claims 12 to 19, wherein a thickness of the second charge trap layer is smaller than a thickness of each of
15 the first charge trap layers in a second direction, wherein the second direction is substantially parallel to the top surface of the substrate.