

Description

This invention as defined in claim 1 relates generally to the field of interface circuits for controlling two-way communication between a keyboard and a data processing system and, more particularly, to a self-pacing interface which permits such communication using only two wires between the interface and the keyboard.

Keyboard entry control circuits or interfaces are generally wellknown in the prior art; however, they are quite complex and require more than two wires between the keyboard and the interface, including, in addition to two wires for carrying clock and data signals, respectively, status lines for indicating the statuses of the keyboard and central processing unit, respectively. Representative prior art keyboard entry control circuits and interfaces are disclosed in the following United States patents: 3,501,749; 3,533,078; 4,038,640; 4,044,398; 4,126,898 and 4,170,768.

US-A-3 980 994 (YING) describes a keyboard with a less complex interface, but this interface does not support two-way communication between the keyboard and the central processing unit.

The present invention eliminates the need for the complex keyboard interface of the prior art while, at the same time, requiring only two wires between the interface and the keyboard. The novel interface of the invention provides the following features:

1. Keyboard data rate and clocking are not tied to any specific clock frequency, and data may be sent at any rate.

2. The only timing relationships required are set-up and hold time required with respect to the rising edge of the keyboard clock; thus, such relationships are easy to implement in microcode.

3. Capability of supporting two-way communications between the keyboard and central processing unit (CPU) of the data processing system.

4. Full handshake and synchronous operation.

5. Relatively few components as compared to prior art interfaces.

The presence of one or the other of two voltage levels on the two lines connecting the keyboard and interface functions to control resetting of the keyboard and transmission of keyboard data.

For a better understanding of the present invention, reference is made to the following description taken in connection with the accompanying drawings, in which:

Figure 1 is a block diagram of a data processing system including the novel interface of the invention.

Figure 2 is a logic block diagram illustrating the details of the novel interface of the invention.

Figure 3 is a timing diagram of the operation of the interface illustrated in Fig. 2.

Fig. 1 is a block diagram of a small computer or data processor, such as a so-called personal computer.

More particularly, a three-state system bus 10,

including address, data and control lines, interconnects the basic components of the computer to provide for the necessary transfer of address, data and control signals among these components. The components include, for example, the central processing unit (CPU) 12, a dynamic random access memory (RAM) 14, a multiple channel programmable direct memory access (DMA) controller 16, an interrupt controller 18, a readonly storage (ROS) 20, digital input/digital output interface (DI/DO) 22, a display adapter 24, a disk adapter 26 and a keyboard interface 28.

A cathode ray tube display device 30 may be connected by a cable 32 to the display adapter 24. A pair of diskette drives 34 and 36 may be connected by a cable 38 to the disk adapter 26. A keyboard 40 is connected by a cable 42 to the keyboard interface 28.

In this preferred embodiment, the CPU 12 is an Intel microprocessor 8088 which is fully disclosed in "The 8086 Family User's Manual, October 1979", published by Intel Corporation, Santa Clara, California. The DMA controller is an Intel 8237 high performance programmable DMA controller also fully disclosed in the above Intel Corporation publication. RAM 14 is any conventional dynamic memory, such as a TI 4116. Interrupt controller 18 is an Intel 8259 chip. ROS 20 is also conventional and may be a Mostek MK 3600, for example. DI/DO 22 is a digital input/digital output interface, such as an Intel 8255A general purpose programmable peripheral interface chip.

Keyboard interface 28 is the subject of the present invention and is illustrated in detail in Fig. 2.

Keyboard 40 is a programmable self-scanning serialized keyboard which transmits a scan code of 8 series data bits identified in the various key positions. The scan code also includes a start bit; thus, each serial scan code is contained in a 9-bit frame headed by the start bit. Also, in the preferred embodiment keyboard 40 is of the capacitive matrix type and has 83 key positions. The keyboard contains its own microprocessor, such as an Intel 8048, and has an OUT CLOCK line, a SENSE CLOCK line, an OUT DATA line and a SENSE DATA line. Furthermore, each key is capable of make/break and typamatic operation. The keyboard contains self-scanning logic and interface controls which will support the protocol for keyboard interface 28, which protocol is described below.

Keyboard 40, itself, forms no part of the present invention and its circuits and construction are found in European Patent application No. 80 103 548.6 filed on June 24, 1980 and in the following U.S. patents: 3,786,497; 3,921,167; and 4,118,611; all of which are incorporated herein by reference.

In general, keyboard interface 28 is self-clocked or self-paced in that it is clocked or paced by the transmission of the keyboard clock and data, completely independently of any other clock rates

in the computer or data processing system. When either the system bus is sending a reset command to the keyboard upon power-up or else the interface has not processed a previous scan code frame, the keyboard is prevented by its control logic from transmitting data. When a complete scan code frame has been stored in the interface, a latch is set to generate an INTERRUPT REQUEST to the CPU via the interrupt controller. When the INTERRUPT REQUEST is granted and data is transferred to the CPU, the latch is cleared or reset to signal the keyboard via its data line that another scan code may be transmitted to the interface. Only two lines are required in the cable connecting the interface and the keyboard in order to perform all of the data, clocking and status sensing functions.

More particularly, and as illustrated in Fig. 2, the SENSE CLOCK line 50 is tied to the keyboard OUT CLOCK line 52 at junction 54, and an open-collector (OC) gate 56 (such as an SN 7407 shown in Texas Instruments' "The TTL Data Book", second edition, 1976) is connected in the OUT CLOCK line 50 between the keyboard control logic and the junction 54. Furthermore, the keyboard SENSE DATA line 57 is tied to the OUT DATA line 58 at the junction 60, and another open-collector (OC) gate 61 is connected in the OUT DATA line between junction 60 and the keyboard control logic. Cable 42, containing only the CLOCK line 52 and the DATA line 58, connects keyboard 40 to the novel keyboard interface 28.

Interface 28, itself, requires only four wires: the keyboard CLOCK and DATA lines, a +5 volt (+5V) and a ground (GND) or zero volt line.

Interface 28 contains a serial-to-parallel shift register (74LS299) encoder 62 having a CLOCK terminal 64 and a SERIAL IN terminal 66 for receiving the serial scan code frame on the DATA line 58 from keyboard 40. Encoder 62 has nine stages and eight corresponding parallel DATA output lines, labeled A, B, ..., E, H and a start line, labeled h'. Stage A is the lowest ordered or least significant stage, and stage h' is the highest ordered or most significant stage. The most significant stage output line h' is connected to the data (D) input terminal of a D-type edge-triggered latch 68. CLOCK line 52 is connected to the clock (CLK) terminal of latch 68. The Q or set output terminal of latch 68 is connected to the system bus 10 and transmits an INTERRUPT REQUEST signal to the CPU 12 via the interrupt controller 18. The $\bar{Q}$ or reset output line of latch 68 is connected through another open-collector (OC) gate 70 to the keyboard DATA line 58. The CLR or reset terminal of latch 68 is also connected to the system bus 10 and receives a CLEAR or reset signal from the CPU when an INTERRUPT REQUEST has been granted and the eight parallel data bits have been transmitted from encoder 62 via D/DO 22 to a register in the CPU.

The OC gates 56, 61 and 70 are functionally switches which, when closed, place ground or a zero (0) voltage on the line to which their outputs are connected. In other words, if a 1 or UP level

appears on a gate input, then the gate output is a 1 (+5V) or UP.

Now, the operation and protocol of keyboard interface 28 will be described with reference to Fig. 2 and the timing diagram of Fig. 3.

First, both the CLOCK line 52 and the DATA line 58 are tied to +5 volts potential on the line will be referred to as the UP state of the line, whereas the existence of 0 or ground potential on a line will be referred to as the DOWN state.

When a key is depressed on keyboard 40, both the OUT CLOCK and OUT DATA are generated. Initially the keyboard sets its OUT CLOCK to a 1. The keyboard then tests or senses the CLOCK line 52 via the SENSE CLOCK line 50 to determine whether the CLOCK line is UP or DOWN. If the CLOCK line 52 is DOWN, the system is requesting keyboard 40 to execute a reset by virtue of a ground signal (RESET) from D/DO 22 on the reset line 72. This condition can occur upon powerup, and causes the keyboard to reset all of its circuits. However, if the keyboard senses an UP state on CLOCK line 52, then keyboard 40 is enabled and tries to raise the DATA line 58.

The keyboard tests or senses DATA line 58 via the SENSE DATA line 56. If the DATA line 58 is DOWN, then the computer or data processing system has not processed the previous scan code which had been transmitted to the interface 28 (and the $\bar{Q}$ output of latch 62 is still DOWN or 0). Thus, the keyboard is disabled and waits for the DATA line 42 to go to 1 or UP. When, or if, DATA line 58 is UP, then keyboard 40 transmits via line 58 a nine-bit frame beginning with a start bit followed by eight series DATA bits representing the scan code identifying a particular key position of the keyboard.

As shown in Fig. 3, the start and eight-data bits are clocked or shifted into the nine-stage encoder 62 under the control of the keyboard OUT CLOCK. Note that the OUT CLOCK is not necessarily periodic, but that the data bits track the OUT CLOCK; thus, interface 28 is not tied to any specific clock frequency within the system; but rather is paced by the keyboard 40. During the transmission of the scan code frame via DATA line 58, interface 28 is under the control of the keyboard 40, and latch 68 is in its cleared or reset state with its $\bar{Q}$ output UP whereby DATA line 58 also UP.

However, when all nine bits of the scan code frame have been shifted or clocked into the encoder 62, the start bit in the most significant stage is clocked by the OUT CLOCK to the D input of latch 48, thereby setting the latch, raising the Q output to send the INTERRUPT REQUEST to the system bus, and lowering the $\bar{Q}$ output, thus applying ground potential to DATA line 56 and causing the DATA line to go DOWN; since the keyboard will sense by its SENSE DATA line 56 the DOWN condition of DATA line 58; the keyboard is prevented from transmitting any additional data. However, after the INTERRUPT REQUEST has been granted and the eight data bits transmitted in parallel from the encoder via

DIDO 22 to the system bus 10, a CLEAR signal from the CPU is applied to the CLR terminal of latch 68, thereby clearing or resetting the latch to cause the $\overline{Q}$ output to go UP and permitting DATA line 58 to return to the UP state which is sensed by the keyboard SENSE DATA line 56 to permit the next scan code frame to be transmitted to the interface 28.

Claims

1. Self-pacing serial keyboard interface for data processing system of the type including a system bus (10) for transferring address, data and control signals among a central processing unit (12), a memory (14) and a self-scanning serial keyboard (40), all connected to the bus, said keyboard having a clock line (52) for transmitting a keyboard out clock signal and a data line (58) for transmitting a serial scan out code in a frame headed by a start bit followed by a predetermined number of serial data bits identifying a key position, said interface providing two-way communication between the bus and the keyboard and comprising:

serial-to-parallel shift register encoder means (62) for storing in parallel the frame of serial bits under the control of the keyboard-out clock signal and having (1) a clock terminal (64) connected to said keyboard clock line, (2) a serial data input terminal (66) connected to said keyboard data line, (3) a number of parallel output data lines A to H corresponding to said predetermined number of data bits, connected to the bus, and (4) a control line h' coupled to the most significant stage of said encoder, said encoder having the same number of stages as the number of bits in a frame, whereby, when said encoder contains said start bit signal and said predetermined number of data bits, a control signal is produced on said control line; and

control means (68), responsive to said control signal and to said keyboard out clock signal, for applying a central processing unit interrupt signal to the bus said control means being further adopted for applying to said data line a disabling signal which prevents further transmission of data bits by the keyboard.

said control means also being responsive to a clear signal from the central processing unit to remove the disabling signal from the data line when said data bits have been transferred from said encoder means to said bus, thereby permitting transmission of another scan code frame from the keyboard to said encoder means.

2. An improved interface as defined in Claim 1 wherein said control means comprises a D-type edge-triggered latch (68) having its D input terminal connected to said control line, its clock terminal connected to said clock line, its $\overline{Q}$ set output terminal connected to the bus, its $\overline{Q}$ reset output terminal connected to said data line, and its clear terminal connected to the bus, whereby said control signal sets said latch to generate said interrupt signal on said $\overline{Q}$ output terminal and

said disabling signal on said $\overline{Q}$ reset output terminal when an entire scan code frame is stored in said encoder, said clear signal being applied to said clear terminal to reset said latch and cause said $\overline{Q}$ reset output terminal to remove said disabling signal from said data line.

3. An improved interface as defined in Claim 2 further comprising means (72), connected to the bus, for applying to said clock line a disabling signal to disable the out clock signal and to reset the keyboard.

4. An improved interface as defined in Claim 3 further comprising gate means (70), coupled between said data line and said $\overline{Q}$ reset output terminal, responsive to said disabling signal for applying ground potential to said data line.

Patentansprüche

1. Schnittstelle eines testenbetaetigten selbstgetakteten seriellen Dateneingabesystems fuer eine Datenverarbeitungsanlage mit einem Sammelbus (10), der zur Verteilung von Adress-, Daten- und Steuersignalen zu einer Zeitraineinheit (12), einem Speicher (14) und einer seriellen Selbstabtast-Tastatur (40) dient, wo die saemtliche Einheiten an dem Sammelbus gekoppelt sind, wobei die Tastatur eine Taktleitung (52) zur Lieferung eines Taktsignals aus der Tastatur und eine Datenleitung (58) zur Lieferung von einem seriellen Abtastkode in einem Rahmen aufweist, der mit einem von einer verbestimmten Anzahl von seriellen Datenbits fuer die Identifizierung einer Taste gefolgten Startbit beginnt, wobei die Schnittstelle Dateneuebermittlung in beiden Richtungen zwischen dem Sammelbus und der Tastatur ermoeeglicht und folgendes auch einschliesst:

Kodiermittel (62) mit seriell-parallelem Verschieberegister, die den Rahmen mit den seriellen Bits in Abhaengigkeit von der Steuerung des aus der Tastatur stammenden Taktsignals parallel speichern und 1) einen mit der Tastatur-Taktleitung verbundenen Takt-Anschluss (64), 2) einen seriellen mit der Tastatur-Datenleitung verbundenen Dateneingangs-Anschluss (66), 3) eine Vielzahl von parallelen der verbestimmten Anzahl von Datenbits entsprechenden und mit dem Sammelbus verbundenen Datenausgangs-Leitungen A bis H und 4) eine mit der Hauptstufe der Kodiermittel verbundene Steuerleitung h' einschliessen, wobei die Kodiermittel die gleiche Anzahl von Stufen wie die Anzahl von in einem Rahmen vorliegenden Bits haben, und wobei ein Steuersignal der Steuerleitung zugefuehrt ist, wenn die Kodiermittel das Startbit-Signal und die vorbestimmte Anzahl von Datenbits aufweisen; und

Steuermittel (68), die auf das Steuersignal und das aus der Tastatur stammende Taktsignal zur Uebergabe eines Zentraleinheit-Unterbrechungssignals zum Sammelbus ansprechen, wobei diese Steuermittel weiterhin so eingestellt sind, dass sie der Datenleitung ein Ausschalt-Signal zufuehren, das die weiteren Uebergabe der Datenbits wegen der Tastatur

DI/DO 22 to the system bus 10, a CLEAR signal from the CPU is applied to the CLR terminal of latch 68, thereby clearing or resetting the latch to cause the $\bar{Q}$ output to go UP and permitting DATA line 58 to return to the UP state which is sensed by the keyboard SENSE DATA line 56 to permit the next scan code frame to be transmitted to the interface 28.

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1. Self-pacing serial keyboard interface for data processing system of the type including a system bus (10) for transferring address, data and control signals among a central processing unit (12), a memory (14) and a self-scanning serial keyboard (40), all connected to the bus, said keyboard having a clock line (52) for transmitting a keyboard out clock signal and a data line (58) for transmitting a serial scan out code in a frame headed by a start bit followed by a predetermined number of serial data bits identifying a key position, said interface providing two-way communication between the bus and the keyboard and comprising:

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control means (68), responsive to said control signal and to said keyboard out clock signal, for applying a central processing unit interrupt signal to the bus said control means being further adopted for applying to said data line a disabling signal which prevents further transmission of data bits by the keyboard.

said control means also being responsive to a clear signal from the central processing unit to remove the disabling signal from the data line when said data bits have been transferred from said encoder means to said bus, thereby permitting transmission of another scan code frame from the keyboard to said encoder means.

2. An improved interface as defined in Claim 1 wherein said control means comprises a D-type edge-triggered latch (68) having its D input terminal connected to said control line, its clock terminal connected to said clock line, its Q set output terminal connected to the bus, its $\bar{Q}$ reset output terminal connected to said data line, and its clear terminal connected to the bus, whereby said control signal sets said latch to generate said interrupt signal on said Q output terminal and

said disabling signal on said $\bar{Q}$ reset output terminal when an entire scan code frame is stored in said encoder, said clear signal being applied to said clear terminal to reset said latch and cause said $\bar{Q}$ reset output terminal to remove said disabling signal from said data line.

3. An improved interface as defined in Claim 2 further comprising means (72), connected to the bus, for applying to said clock line a disabling signal to disable the out clock signal and to reset the keyboard.

4. An improved interface as defined in Claim 3 further comprising gate means (70), coupled between said data line and said $\bar{Q}$ reset output terminal, responsive to said disabling signal for applying ground potential to said data line.

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1. Schnittstelle eines testenbetaetigten selbstgetakteten seriellen Dateneingabesystems fuer eine Datenverarbeitungsanlage mit einem Sammelbus (10), der zur Verteilung von Adress-, Daten- und Steuersignalen zu einer Zeitraineinheit (12), einem Speicher (14) und einer seriellen Selbstabtast-Tastatur (40) dient, wo die saemtliche Einheiten an dem Sammelbus gekoppelt sind, wobei die Tastatur eine Taktleitung (52) zur Lieferung eines Taktsignals aus der Tastatur und eine Datenleitung (58) zur Lieferung von einem seriellen Abtastkode in einem Rahmen aufweist, der mit einem von einer verbestimmten Anzahl von seriellen Datenbits fuer die Identifizierung einer Taste gefolgten Startbit beginnt, wobei die Schnittstelle Dateneuebermittlung in beiden Richtungen zwischen dem Sammelbus und der Tastatur ermoeoglicht und folgendes auch einschliesst:

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Steuermittel (68), die auf das Steuersignal und das aus der Tastatur stammende Taktsignal zur Uebergabe eines Zentraleinheit-Unterbrechungssignals zum Sammelbus ansprechen, wobei diese Steuermittel weiterhin so eingestellt sind, dass sie der Datenleitung ein Ausschalt-Signal zufuehren, das die weiteren Uebergabe der Datenbits wegen der Tastatur



verhindert, wobei diese Steuermittel auch auf ein Loesch-Signal aus der Zentraleinheit zur Entfernung des Ausschalt-Signals aus der Datenleitung ansprechen, wenn die Datenbits aus den Kodiermitteln zum Sammelbus uebergeben worden sind, so dass die Uebergabe von einem anderen Abtastkode-Rahmen aus der Tastatur zu den Kodiermitteln erfolgen kann.

2. Verbesserte Schnittstelle nach Anspruch 1, in der die Steuermittel einen Trigger-Schalter des Typs D (68) aufweisen, dessen D-Eingangsanschluss mit der Steuerleitung, dessen Takt-Anschluss mit der Taktleitung, dessen Q-Einsetz-Ausgangsanschluss mit dem Sammelbus, dessen Q-Ruecksetz-Ausgangsanschluss mit der Datenleitung, und dessen Loeschsignal-Anschluss mit dem Sammelbus verbinden ist, wobei das Steuersignal den Trigger-Schalter zur Lieferung des Unterbrechungssignals zum Q-Ausgangsanschluss und zur Leifereung des Ausschalt-Signals zu dem Q-Ruecksetz-Ausgangsanschluss steuert, wenn ein ganzer Abtastkode-Rahmen in den Kodiermitteln eingespeichert ist, wobei das Loeschsignal dem zugehoerigen Anschluss zum Ruecksetzen des -Trigger-Schalters zugefuehrt ist, und dazu fuehrt, dass der Q-Ruecksetz-Ausgangsanschluss die Entfernung des Ausschalt-Signals aus der Datenleitung steuert.

3. Verbesserte Schnittstelle nach Anspruch 2, die weiterhin mit dem Sammelbus verbundene Mittel (72) aufweist, die der Taktleitung ein Ausschalt-Signal zum Ausschalten des Ausgangs-Taktsignals und zum Ruecksetzen der Tastatur zufuehren.

4. Verbesserte Schnittstelle nach Anspruch 3, die weiterhin zwischen der Datenleitung und dem Q-Ruecksetz-Ausgangsanschluss gekoppelte Gate (70) aufweist, die auf das Ausschalt-Signal ansprechen, um der Datenleitung Erdspannung zuzufuehren.

Revendications

1. Interface sérielle d'un clavier à horloge autonome pour un système de traitement de données du type comprenant un bus de système (10) pour répartir des signaux d'adresse, de données et de commande sur une unité centrale de traitement (12), une mémoire (14) et un clavier de série à balayage autonome (40) tous connectés au bus, ledit clavier ayant une ligne d'horloge (52) pour transmettre un signal d'horloge de clavier, et une ligne de données (58) pour transmettre un code de balayage en série d'une trame commençant par un bit de départ suivi d'un nombre prédéterminé de bits de données en série identifiant une position de touche, ladite interface assurant une communication dans les deux sens entre le bus et le clavier, et comprenant:

un codeur à registres à décalage série-parallèle (62) pour emmagasiner en parallèle la trame de bits en série sous la commande du signal d'horloge du clavier et ayant (1) une borne d'horloge

(64) connectée à ladite ligne d'horloge du clavier, (2) une borne d'entrée de données en série (66) connectée à ladite ligne de données du clavier, (3) un nombre de ligne de données de sortie en parallèle A à H correspondant audit nombre prédéterminé de bits de données, connectées au bus, et (4) une ligne de commande h' couplée à l'étage le plus élevé dudit codeur, ledit codeur ayant un nombre d'étages qui est le même que le nombre de bits d'une trame afin que, lorsque ledit codeur contient ledit signal de bit de départ et ledit nombre prédéterminé de bits de données, un signal de commande soit produit sur ladite ligne de commande, et,

des moyens de commande (68), sensibles audit signal de commande et audit signal d'horloge du clavier, pour appliquer au bus un signal d'interruption de l'unité centrale de traitement, lesdits moyens de commande pouvant en outre appliquer à ladite ligne de données un signal de déconditionnement qui empêche toute autre transmission de bits de données par le clavier, lesdits moyens de commande étant également sensibles à un signal d'effacement provenant de l'unité central de traitement pour supprimer le signal de déconditionnement de la ligne de données lorsque lesdits bits de données ont été transférés dudit codeur audit bus, afin de permettre la transmission d'une autre trame de code de balayage du clavier audit codeur.

2. Interface améliorée selon la revendication 1, dans laquelle lesdits moyens de commande comprennent une bascule à verrouillage de type D (68) ayant sa borne d'entrée D connectée à ladite ligne de commande, sa borne d'horloge connectée à ladite ligne d'horloge, sa borne de sortie d'instauration Q connectée au bus, sa borne de sortie de restauration Q connectée à ladite ligne de données, et sa borne d'effacement connectée au bus, de sorte que le signal de commande instaure ladite bascule pour engendrer ledit signal d'interruption sur ladite borne de sortie Q et ledit signal de déconditionnement sur ladite borne de sortie de restauration Q lorsqu'une trame entière de code de balayage est emmagasinée dans ledit codeur, ledit signal d'effacement étant appliqué à ladite borne d'effacement afin de restaurer ladite bascule à verrouillage et de permettre à ladite borne de sortie de restauration Q de supprimer ledit signal de déconditionnement sur ladite ligne de données.

3. Interface améliorée selon la revendication 2, comprenant en outre des moyens (72) connectés au bus pour appliquer à ladite ligne d'horloge un signal de déconditionnement afin de déconditionner le signal d'horloge du clavier et de rétablir le clavier dans sa condition initiale.

4. Interface améliorée selon la revendication 3, comprenant en outre des moyens de porte (70) couplés entre ladite ligne de données et ladite borne de sortie de restauration Q, sensibles audit signal de déconditionnement pour appliquer le potentiel de masse à ladite ligne de données.

