EEPROM CELL

ABSTRACT

A method of forming a device is disclosed. The method includes providing a substrate prepared with a cell area and forming first and second gates of first and second transistors in the cell area. The first gate includes a second sub-gate surrounding a first sub-gate. The first and second sub-gates of the first gate are separated by a first intergate dielectric layer. The second gate includes a second sub-gate surrounding a first sub-gate. The first and second sub-gates of the second gate are separated by a second intergate dielectric layer. The method also includes forming first and second junctions of the first and second transistors. A first gate terminal is formed and coupled to the second sub-gate of the first transistor. A second gate terminal is formed and coupled to at least the first sub-gate of the second transistor.

Fig. 1a