METHOD TO FORM $CoSi_2$ ON SHALLOW JUNCTION BY Si IMPLANTATION

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to the fabrication of integrated circuit devices, and more particularly, to a method of reducing silicon consumption in the formation of cobalt silicide in the fabrication of integrated circuits.

(2) Description of the Prior Art

Cobalt disilicide ($CoSi_2$) is a preferred salicide technology as CMOS device sizes shrink to 0.18 μm and beyond because of its good performance with small polysilicon and active area line widths. However, $CoSi_2$ is known to consume more Si than does $TiSi_2$. This is a drawback for shallow junctions used in future technologies. It is desired to find a process which will form $CoSi_2$ without increased Si consumption.

U. S. Patent 5,710,438 to Oda et al teaches an ion implant into cobalt before annealing to remove the native oxide film underlying the cobalt layer. U.S. Patent 5,874,342 to Tsai et al teaches using a metal capping layer over cobalt and forming $CoSi_2$ using two annealing steps.

Ions are implanted into the $CoSi_2$ which is heated again to diffuse the ions into the substrate to form S/D regions. U.S. Patent 5,536,676 to Cheng et al implants ions into polysilicon, then deposits cobalt thereover. The substrate is annealed to form both CoSi and junctions under the polysilicon by diffusion of the implanted ions. U.S. Patents 5,824,600 to Byun et al, 5,780,361 to Inoue, and 5,510,295 to Cabral, Jr. et al show various methods of cobalt silicide formation.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method of fabricating a cobalt disilicide film in the fabrication of an integrated circuit.

A further object of the invention is to provide a method of fabricating cobalt disilicide with reduced silicon consumption in the fabrication of an integrated circuit.

Yet another object is to provide a method of forming a cobalt disilicide film on shallow junctions.

Yet another object is to provide a method of forming a cobalt disilicide film on shallow junctions with reduced silicon consumption.

Yet another object of the invention is to forming a cobalt disilicide film on shallow junctions with reduced silicon consumption by implanting silicon ions.

In accordance with the objects of the invention a method for forming a cobalt disilicide film on shallow junctions with reduced silicon consumption in the fabrication of an integrated circuit is achieved. A semiconductor substrate is provided having silicon regions to be silicided. A cobalt layer is deposited overlying the semiconductor substrate and subjected to a first rapid thermal process whereby the cobalt is transformed to cobalt monosilicide where it overlies the silicon regions and wherein the cobalt not overlying the silicon regions is unreacted. The unreacted cobalt layer is removed. A dielectric layer is deposited overlying the substrate and the cobalt monosilicide layer. Silicon ions are implanted through the dielectric layer into the cobalt monosilicide layer. The substrate is subjected to a second rapid thermal process whereby the cobalt monosilicide is transformed to cobalt disilicide wherein the silicon ions implanted into

the cobalt monosilicide layer act as a main (not sole) silicon source for the transformation to complete formation of a cobalt disilicide film in the manufacture of an integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Figs. 1 through 7 schematically illustrate in cross-sectional representation a preferred embodiment of the present invention.

Fig. 8 schematically illustrates in cross-sectional representation a completed integrated circuit manufactured according to the process of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The process of the present invention can be used in any application in which it is desired to form a cobalt disilicide film overlying a silicon region. The process of the invention will be described for the

application in which $CoSi_2$ is formed overlying a gate electrode and source and drain regions. It is to be understood that the invention is not limited to the application so illustrated.

Referring now more particularly to Fig. 1, there is shown an illustration of a portion of a partially completed integrated circuit. The semiconductor substrate 10 is preferably composed of silicon having a (100) crystallographic orientation. Gate electrodes 16 and source and drain regions 20 are formed in and on the semiconductor substrate as is conventional in the art. For example, gate electrode 16 has been formed overlying a gate oxide layer 14. Sidewall spacers, such as silicon oxide, 18 are formed on the gate. Source and drain regions are n-type or p-type, depending on the type of device to be fabricated.

The wafer is subjected to a pre-metal clean, such as a wet clean using hydrofluoric acid (HF), for example. Next, as shown in Fig. 2, a layer of cobalt 24 is sputter deposited over the surface of the substrate and overlying the gate electrode. The cobalt layer has a thickness of between about 50 and 200 Angstroms. Next, a capping metal layer, such as titanium nitride or titanium is deposited over the cobalt layer to a thickness of between

about 100 and 300 Angstroms. The metal capping layer is optional, but preferred. The metal capping layer is used to prevent cobalt oxidation during rapid thermal anneal (RTA), There are other ways to avoid cobalt oxidation, such as high temperature (450 °C) cobalt deposition and/or in-situ anneal. But, the metal cap process is more manufacturable.

Now, the wafer is subjected to a first rapid thermal process (RTP) at a low temperature of between about 500 and 600 °C and preferably of about 550 °C for 20 to 60 seconds. This annealing will form cobalt monosilicide (CoSi) 26 over the gate electrode and over the source and drain regions, as shown in Fig. 3. This low temperature annealing to form CoSi first consumes only 57% of the silicon consumed by an annealing which would form $CoSi_2$. For example, 1 Angstrom of cobalt is transformed to 2.02 Angstroms of CoSi versus 3.52 Angstroms of $CoSi_2$.

Referring now to Fig. 4, the metal capping layer 28 and the unreacted cobalt layer 24 are stripped from the wafer surface, leaving the CoSi film 26 over the gate electrode 16 and the source and drain regions 20.

A dielectric capping film 30 is deposited over the wafer surface, as shown in Fig. 5, to a thickness of

between about 500 and 1000 Angstroms. This capping film 30 may comprise an oxide, nitride, or oxynitride, for example.

Next, silicon ions are implanted into the CoSi layer through the capping dielectric film 30, as shown by 32 in Fig. 6. The implantation is at a high dose of between about $1x10^{16}$ to $1x10^{17}$ atoms/cm^2 and at a energy of between about 10 to 50 KeV. The capping dielectric film serves as a barrier to reduce implant channeling. The thickness of the capping dielectric film can be varied so that the ions will be centered vertically within the CoSi film.

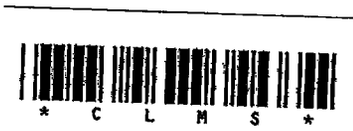
Now, the wafer is subjected to a second RTP, this time at a temperature of between about 750 and 900 °C, to transform the cobalt monosilicide (CoSi) to cobalt disilicide ($CoSi_2$) 34, as shown in Fig. 7. The implanted silicon will be the main silicon source for the conversion of CoSi to $CoSi_2$. Therefore, there will be no or minimal further consumption of silicon from the gate and source and drain regions. This is especially important where there are shallow source/drain junctions.

Standard backend processing continues as is conventional to complete the integrated circuit. The dielectric capping layer 30 may be removed after the silicon

implantation or may remain over the silicide layer as part of the interlayer dielectric. For example, Fig. 8 shows the capping dielectric 30 covered by an additional thick dielectric layer 36. Electrical connections may be made, for example, to one of the silicided source/drain regions 20 by metal contact 40, as shown.

The process of the invention provides an effective method of forming $CoSi_2$ for shallow junctions and small feature sizes by reducing silicon consumption. Forming first CoSi reduces silicon consumption. Then, silicon ions are implanted through a capping dielectric layer to provide a silicon source for the second annealing step to convert CoSi to $CoSi_2$.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.



CLAIMS

1. A method of fabricating a cobalt disilicide film in the manufacture of an integrated circuit comprising:

providing a semiconductor substrate having silicon regions to be silicided;

depositing a cobalt layer overlying said semiconductor substrate;

subjecting said substrate to a first rapid thermal process whereby said cobalt is transformed to cobalt monosilicide where it overlies said silicon regions and wherein said cobalt not overlying said silicon regions is unreacted;

removing said unreacted cobalt layer;

depositing a dielectric layer overlying said substrate and said cobalt monosilicide layer;

implanting silicon ions through said dielectric layer into said cobalt monosilicide layer; and

thereafter subjecting said substrate to a second rapid thermal process whereby said cobalt monosilicide is transformed to cobalt disilicide wherein said silicon ions implanted into said cobalt monosilicide layer act as a silicon source for said transformation to complete formation of said cobalt disilicide film in the manufacture of said integrated circuit.

2. The method according to Claim 1 wherein said silicon regions to be silicided comprise gate electrodes and associated source and drain regions.

3. The method according to Claim 1 wherein said cobalt layer is sputter deposited to a thickness of between about 50 and 200 Angstroms.

4. The method according to Claim 1 further comprising depositing a capping metal layer overlying said cobalt layer.

5. The method according to Claim 4 wherein said capping metal layer comprises one of the group containing titanium and titanium nitride having a thickness of between about 100 and 300 Angstroms.

6. The method according to Claim 1 wherein said first rapid thermal process is performed at a temperature of between about 500 and 600 °C.

7. The method according to Claim 4 wherein said capping metal layer is removed during said step of removing said unreacted cobalt layer.

8. The method according to Claim 1 wherein said dielectric layer comprises one of the group containing silicon oxide, silicon nitride, and silicon oxynitride and wherein said dielectric layer has a thickness of between about 500 and 1000 Angstroms.

9. The method according to Claim 1 wherein said silicon ions are implanted at a dosage of between about $1x10^{16}$ and $1x10^{17}$ atoms/cm^2.

10. The method according to Claim 1 wherein said second rapid thermal process is performed at a temperature of between about 750 and 900 °C.

11. A method of fabricating a cobalt disilicide film in the manufacture of an integrated circuit comprising:

providing a semiconductor substrate having silicon regions to be silicided;

depositing a cobalt layer overlying said semiconductor substrate;

subjecting said substrate to a first rapid thermal process at a low temperature of less than 600 °C whereby said cobalt is transformed to cobalt monosilicide where it overlies said silicon regions and wherein said cobalt not overlying said silicon regions is unreacted;

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removing said unreacted cobalt layer;

depositing a dielectric layer overlying said substrate and said cobalt monosilicide layer;

implanting silicon ions through said dielectric layer into said cobalt monosilicide layer;

thereafter subjecting said substrate to a second rapid thermal process whereby said cobalt monosilicide is transformed to cobalt disilicide wherein said silicon ions implanted into said cobalt monosilicide layer act as a silicon source for said transformation to complete formation of said cobalt disilicide film in the manufacture of said integrated circuit.

12. The method according to Claim 11 wherein said silicon regions to be silicided comprise gate electrodes and associated source and drain regions.

13. The method according to Claim 11 wherein said cobalt layer is sputter deposited to a thickness of between about 50 and 200 Angstroms.

14. The method according to Claim 11 further comprising depositing a capping metal layer overlying said cobalt layer.

15. The method according to Claim 14 wherein said capping metal layer comprises one of the group containing titanium and titanium nitride having a thickness of between about 100 and 300 Angstroms.

16. The method according to Claim 14 wherein said capping metal layer is removed during said step of removing said unreacted cobalt layer.

17. The method according to Claim 11 wherein said dielectric layer comprises one of the group containing silicon oxide, silicon nitride, and silicon oxynitride and wherein said dielectric layer has a thickness of between about 500 and 1000 Angstroms.

18. The method according to Claim 11 wherein said silicon ions are implanted at a dosage of between about $1x10^{16}$ and $1x10^{17}$ atoms/cm^2.

19. The method according to Claim 11 wherein said second rapid thermal process is performed at a temperature of between about 750 and 900 °C.

20. A method of fabricating a cobalt disilicide film in the manufacture of an integrated circuit comprising:

providing a gate electrodes and associated source and drain regions in and on a semiconductor substrate wherein said gate electrodes have dielectric spacers on their sidewalls;

depositing a cobalt layer overlying said gate electrodes and associated source and drain regions;

depositing a capping metal layer overlying said cobalt layer;

subjecting said substrate to a first rapid thermal process at a low temperature of less than 600 °C whereby said cobalt is transformed to cobalt monosilicide where it overlies said gate electrodes and source and drain regions and wherein said cobalt overlying said dielectric spacers is unreacted;

removing said unreacted cobalt layer and said capping metal layer;

depositing a dielectric layer overlying said substrate and said cobalt monosilicide layer;

implanting silicon ions through said dielectric layer into said cobalt monosilicide layer;

thereafter subjecting said substrate to a second rapid thermal process whereby said cobalt monosilicide is transformed to cobalt disilicide wherein said silicon ions implanted into said cobalt monosilicide layer act as a silicon source for said transformation to complete

formation of said cobalt disilicide film in the manufacture of said integrated circuit.

21. The method according to Claim 20 wherein said cobalt layer is sputter deposited to a thickness of between about 50 and 200 Angstroms.

22. The method according to Claim 20 wherein said capping metal layer comprises one of the group containing titanium and titanium nitride having a thickness of between about 100 and 300 Angstroms.

23. The method according to Claim 20 wherein said dielectric layer comprises one of the group containing silicon oxide, silicon nitride, and silicon oxynitride and wherein said dielectric layer has a thickness of between about 500 and 1000 Angstroms.

24. The method according to Claim 20 wherein said silicon ions are implanted at a dosage of between about $1x10^{16}$ and $1x10^{17}$ atoms/cm^2.

25. The method according to Claim 20 wherein said second rapid thermal process is performed at a temperature of between about 750 and 900 ^oC.