

It is known with devices according to the preamble of claim 1, to select the individual signal sources for further signal processing by preselection by means of a manually operated switch. This has the disadvantage that in each recording or reproduction procedure the selection has to be carried out again by the operator.

The object of the invention is to provide the possibility of selecting the signal sources without operating a selector switch in the case of different digital and analog signals being available at the individual input terminals of, for example, a DAT-device (digital audio tape).

According to the invention the object is achieved by the features set out in claim 1. Further developments of the invention are characterised in the dependent claims.

In principle, the input terminal for further signal processing is selected by a detector unit in the device according to a predefined priority schedule. The detector unit is controlled by a microprocessor in which the priority schedule for the selection of the existing input terminals is programmed or programmable. At the input terminals the following signals can be selected, for example, in a DAT-device:

1. digital signal, transmission by light guide,
2. digital signal, transmission by cable.
3. analog signal, transmission by cable.

The digital signals have TTL-level and are bi-phase coded, as defined in STANDARD AND INFORMATION DOCUMENTS AES 3-1985 (ANSI S4.40-1985). The possible clock frequencies are 32 kHz, 44.1 kHz, and 48 kHz.

Out of several available signals, the signal is selected which has the highest priority according to the priority schedule. If the detector circuit recognises an evaluable signal, this connection state is maintained, that is, this signal is used for further processing in the device. For reasons of quality, this may be the signal which is distributed by the optic cable, but it may also be any other available signal according to the predefined priority.

In the following the invention will be explained in more detail with reference to an embodiment.

Fig. 1 shows a block diagram for the automatic selection of the signal source,

Fig. 2 shows a block diagram of the identification electronics unit for the selection of digital input signals.

In Fig. 1 three different input sources with the allocated

input terminals are shown. The input terminal 1 is provided for a digital signal fed by an optical conductor, the input terminal 2 for a digital signal fed by a cable, and the input terminal 3 for an analog signal. The signals available at the input terminals 1 and 2 are fed through the amplifier 4 or 5 to the input unit a or b of the decoder circuit 7, while the analog from terminal 3 is fed via an A/D-converter 6 to the decoder circuit 7 at connection c. The decoder circuit 7 is controlled by a microprocessor 8 via the connections f and g, according to a program stored in the microprocessor with a stored priority schedule. The microprocessor 8 is connected to an indicator unit 9 by the connection h.

The decoder 7 contains an identification electronics unit K and an electronic switch Q. If, for example, the selection of a digital signal for the further signal processing 16 is defined as priority in the priority schedule, the connection e of switch Q, controlled by connection g, is connected by line d to the identification electronics unit K. Another criterion, given out from the microprocessor through connection f, is the definition which of the possibly available digital signals is the first to be selected. This is carried out by the selector switch S in the identification electronics circuit K, which is shown in detail in Fig. 2. The connection f, connecting the microprocessor 8 and the identification electronics circuit K, consists of different lines f1 - f6 via which information is exchanged. Thus, the selector switch S is controlled through the line f1 and the lock-in range for the PLL-circuit 10 in the identification electronics circuit is controlled through the lines f2, f3, and f4. The lines f5 and f6 give information on the current state from the identification electronics circuit K back to the microprocessor 8, which is also displayed in the indicator panel 9.

The identification electronics circuit K consists of the following circuit parts: The inputs for the digital signals a and b are selected by means of an electronically controlled switch S. The selected signal is fed on the one hand to the PLL-circuit 10 and on the other hand to a bi-phase decoder 13. The PLL-circuit is connected to an oscillator circuit 11, the frequencies of which can be selected by the microprocessor 8 through the programmable frequency divider 12 through the lines f2 - f4 according to the expected clock frequencies of the digital signals to be selected.

The output of the PLL-circuit is connected to the microprocessor 8 by the line f5 and gives a back indication to the microprocessor 8 if a digital signal is locked on one of the predefined frequencies. This back indication stops the microprocessor in its selection program, that is, the locked state of the identification electronics circuit K is maintained. The audio-data signal decoded in the bi-phase decoder 13 is supplied to the signal processing unit 16

through the isolation stage 14 with output unit d and the source switch Q, connected in series. Besides, the signal from the output of the bi-phase decoder 13 is fed to an isolation stage 15 for the subcode data contained in the signal. These subcode data are transmitted via line f9 for the display in the indicator panel 9. These data are processed in the microprocessor 8.

The procedure of signal selection according to a priority schedule defined in the microprocessor is as follows:

1. Definition of the connection state of switch Q by the priority schedule (digital input or analog input).
2. With digital input selected, adjustment of the lock-in range of PLL 10 by definition of the clock frequencies of the digital signal to be expected according to the priority schedule.
3. Locking of PLL 10 on the clock frequency of a present digital signal.
4. Termination of the selection program via line f5 and processing of the selected signal in the device.

After termination of the source selection the connection state is maintained until a new selection procedure is started, for example, by entry of an instruction through remote control. A new selection procedure can also be started automatically through the microprocessor in case of outage of a connected signal source.



CLAIMS

1. A recording and reproduction device with a processor-controlled selection circuit for a signal to be recorded from a plurality of source signals supplied to the device, characterised in that the device has a switching and detector unit (7), to which are supplied the source signals (a,b,c) as well as control signals (g, f_1-f_4) of a microprocessor (8) connected to the switching and detector unit, in which by means of the control signals ($g, f_1 - f_4$) a source signal can be selected according to a priority schedule for the source signal selection, controlled by the program of the microprocessor, in which a detection signal (f_5) supplied to the processor (8) is generated by means of a PLL circuit (10 - 12) having a switchable frequency and provided in the switching and detector unit by locking of the PLL circuit to the clock frequency of a selected digital source signal, upon which the program is stopped by the processor and the corresponding source signal selection is maintained.
2. A device according to claim 1, characterised in that the lock-in range of the PLL circuit (10) is switchable to discrete fixed frequencies ($f_2 - f_4$).
3. A device according to claim 1, characterised in that the lock-in range of the PLL circuit (10) embraces the clock frequencies of all the digital sources which can be processed.
4. A device according to claim 1, characterised in that analog signal sources may be connected via separate input terminals (3), the signals of which are converted in the device into digital signals.
5. A device according to any one of claims 1 - 4, characterised in that when the PLL circuit (10) is not locked-in, an analog signal source is selected for the signal processor.
6. A device according to any one of claims 1 - 5, characterised in that after termination of the source selection, this state is changed upon outage of the selected signal source.
7. A device according to any one of claims 1 - 5, characterised in that the current state of a selected source is stored by the microprocessor (8).
8. A device according to any one of claims 1 - 5, characterised in that all occurring signal sources are selected in turn, and in that the respective state of the individual sources is stored.
9. A device according to claim 8, characterised in that the state of a selected or of all sources stored in the microprocessor (8) is indicated in the display unit (9).